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Investigation and Design of High Efficiency Quadrature Power Amplifier for 5G Applications

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ABSTRACT

The rapid rise of the high data rate requirements in modern wireless communications, which include Wi-Fi, LTE, and 5G, demands that appropriate linear and efficient transmitter architecture gets designed. The increased power amplifier (PA) efficiency in the output power back-off (OPBO) is one of the major challenges because it is difficult to achieve PA power efficiency and linearity at the same time. The current study provides design and simulation of a Quadrature Power Amplifier (QPA) for application in 5G in the 5.8 GHz band using 120nm CMOS technology. The proposed QPA system combines Envelope Elimination and Restoration (EER) technique with direct I and Q signal modulation, quite a different solution from the "conventional" approaches of EER and represents very a bandwidth efficient one. Hard-switching drivers as well as the optimized matching networks are used by the system to ensure that there is high power transfer capability and low distortion. In the design process the source impedance is optimized using a source pull simulation and the load impedance is optimized by using a load pull simulation; then, the L-type network is designed to realize optimal matching. For use in implementation, the Rogers RO-5880 material is applied using transmission lines set up through the microstrip techniques in a bid to reduce the losses and parasitic ones. Simulation results show that the QPA obtains a peak output power of 24.35dBm and a power-added efficiency (PAE) of 70% at 5.8 GHz. The best input and output impedances were: $(2.929 + j8.349)\,\Omega$ and $(18.252 + j19.015)\,\Omega$, respectively. In addition, the envelope and transient simulations prove high-accuracy signal transmission and clean switching quality. This QPA design offers a power-efficient solution with better performance characteristics that makes it an attractive candidate for the future 5G communication systems that are to operate in the 5.8 GHz frequency band.

1. Introduction

The fast evolution of contemporary wireless communication systems including Wi-Fi, LTE, and 5G, require the development of the technologies of transmitters that can provide high data rates, outstanding accuracy, linearity, and energy efficiency, respectively. An extremely important point in this regard is the optimization of the power amplifier's (PA's) power efficiency especially at the point of Output Power Back-Off (OPBO), where efficiency of the PA has a direct impact on the reduction of RF power consumption. Two key restraints in amplifier controller design are high efficiency and linearity that must be balanced judiciously against the stringent requirements of the next generation wireless systems [1].

Of many parts of a transmitter, the power amplifier (PA) is arguably one of the most important, parameterizing the linearity, dynamic range of the output power, power consumption, and signal quality [2]. The design and manufacturing of a PA are largely determined by target operating frequency and output power, and it is subject to multiple challenges, such as high gain, linearity and both fabrication and chip area costs, along with power consumption [3]-[4].

Several methods have been formulated over the years to produce more efficient PAs. They are as follows: Doherty Power Amplifiers (DPA) [5], envelope tracking [6], Class J PA [7], Class E PA [8], Class F PA [9], and load modulation [10]. Other materials have also been considered for PA fabrication such as LDMOS [11], GaN [12] and CMOS technologies [13]. Of these, CMOS technology has become the ideal choice of technology for ICs owing to reduced cost and simplicity of fabrication process [14]. But CMOS technology always has difficulty in gathering the high output power, and there is always an inherent compromise between linearity and efficiency [25]-[27].

Message signal in the modem RF transmitter goes through filtering, digital to analog conversion, signal processing. Signal amplification is the last step in converting baseband signals to radio frequency (RF) frequencies, and it is a critical step since it contributes extensively to high efficiency and excellent linearity achieved in these systems [28]-[33]. Traditionally, switched mode PA such as class D PA show high efficiency at high frequencies but they are constrained by their need to work with constant envelop signal hence not suitable for a wider range of modern communication scheme. In response to the demands of increasing high-data-rate transmission demands, there is a new trend among the different modulation schemes, for example, quadrature modulation [34]-[37]. The quadrature modulation produces signals that have variable envelopes alleviating the peak-to-average power ratio problem that exists in non-constant envelope systems [15] and [24].

These notable contributions to the field are those put forward a proposal of an envelope power amplifier (EPA) according to envelope elimination and restoration (EER) of wireless LAN applications [38]-[44]. At a frequency of operation: 2.4 GHz, this design proved high efficiency and wide bandwidth, while reaching 28% power-added efficiency (PAE) and 19 dBm Output Power [6]. Based on a 10W GaN HEMT transistor have published a DPA design by more recent research (2022) for 5G application of which, PAE 70% has been achieved (in the frequency range of 2-3 GHz) along with a saturated output power of 44 dBm [16]. Presented a novel quadrature power amplifier (QPA) design which excels over conventional polar PAs that use the EER linearizing method in the range of 2.4 GHz with a 90-nm CMOS process with a PAE of approximately 30% [17].

This work contributes a new method in designing and simulating nonlinear Quadrature Power amplifier (QPA) with GaAs 0.12µm CMOS technology, to produce 5G frequency bands like 5.8 GHz [45]-[50]. Proposed QPA design uses EER linearization technique and adds switch-mode PAs in QPA configurations. Such a configuration enables direct amplification of the signal without decomposition into the phase and amplitude components leading to improved efficiency. The simulated results show that the proposed QPA can deliver up to a high output power (24.35 dBm) and power-added efficiency (PAE) of 70 % at an RF input power of 20 dBm [51]-[54]. This performance shows the promise of the QPA to solve the problems of efficiency and linearity in next-generation communication systems.

The major contribution of this work is the designing and simulation of a modern design for quadrature power amplifier (QPA) in GaAs 0.12µm CMOS technology [55]-[60]. This study presents

a new technique for improving power efficiency and linearity of RF transmitters used in 5G applications. Unlike conventional designs for amplifier circuits, the proposed QPA design efficiently accommodates non-constant envelop signals, addressing the issues of conventional Class D and other switched-mode amplifiers. Further research shows how the proposed QPA can realize substantial improvements in terms of both output power and power-added efficiency, making it a promising candidate for future wireless communication systems.

The following parts of this manuscript will describe the QPA design itself, how it uses, the simulation results, and a comparison to available amplifier technologies to show the novelty and the possible impact of the approach considered. The organization of the rest of this paper is as follows: The method and circuit design are outlined in Section 2, while in Section 3 the simulation results and performance analysis are discussed, Section 4 concludes the study and promotes future directions.

2. Quadrature Power Amplifier Circuit Design

The quadrature configuration of the power amplifier (PAs) is used to directly amplify and modulate the quadrature signals, instead of analyzing these signals in a set of phases and amplitude. Because of the lack of separate modulated signals, the linearity and bandwidth requirements of PAs design is not satisfied. Therefore, quadrature QPAs is one possible way to overcome these problems using an envelope elimination and recombination (EERs) technique. The general form of the modulated signal is described as (1) [17]:

$$V_{RF}(t) = A(t)\sin(\omega t + \emptyset(t)) \tag{1}$$

The modified signal can be written as follows (2):

$$V_{RF}(t) = A(t)\,[cos(\omega t)\ cos\ (\emptyset(t) - sin(\omega t)\ sin\ (\emptyset(t)] \tag{2}$$

Where the $A(t), \emptyset(t)$ are the amplitude and phase of the modulated RF signal respectively, it is seen from (2) that there are two modified quadratic functions are sine and cosine. The message signals I(t) and Q(t) are mixed by a local oscillator with a phase shift of 90 degrees compared to each other and it can be determined by (3) and (4) respectively. So, the (2) can be rewritten as in (5) followed using subtraction of two modulated quadrature signals [17].

$$I(t) = A(t)\cos\,(\emptyset(t)) \tag{3}$$

$$Q(t) = A(t)\sin(\emptyset(t)) \tag{4}$$

$$V_{RF}(t) = I(t)\cos(\omega t) - Q(t)\sin\,(\omega t) \tag{5}$$

The general block diagram of the quadrature power amplifier system is shown in Fig. 1 (a). It consists of two quadrature modulated RF signals separated by 90° phase difference in bridge mode unlike conventional Envelope Elimination and Restoration EER technique. As a result, each power amplifier (PA) is driven by a fixed amplitude, phase, vector, and voltage source that is modulated by message signals I(t) or Q(t). The RF modulated signal (VRF(t)) is provided by two quadrature signals that separated by 90 phase shift between them and it's shown in Fig. 1 (b) [17].

Unlike with classic EER technique, the quadrature configuration of the power amplifier removes the requirement for adapting the envelope to the phase path. Furthermore, a wideband envelope path is unnecessary. Because of this, the signal bandwidth in a quadrature PA system, which is based on the quadrature signals I(t), and Q(t), is substantially smaller than the envelope modulator's restricted bandwidth in an EER system.

It is seen from Fig. 1 (a) that the QPAs system consists of two power amplifiers (PAs) for both positive and negative supply voltage modulation. The PA modulates the RF carrier signal using the quadrature signals I(t), and Q(t). There are two modes of choice of the PA configuration in the QPA system, first of them the linear mode such as Class A, AB, B and secondly nonlinear modes of PAs

such as Class D, or E. It is impossible to use linearity because the output current is not a direct linear function of the voltage source and has the characteristics of a current source. Therefore, the simplest way to achieve this is to use a switched mode PA system [18]. Class E PA has higher efficiency compared to Class D, but it is unusable in a quadrature configuration. So, in this work the D PA has been choice in a QPA system due to its high efficiency, and its driving by a hard switch operates at the frequency of 5.8 GHz, and the duty cycle is 50% [19].

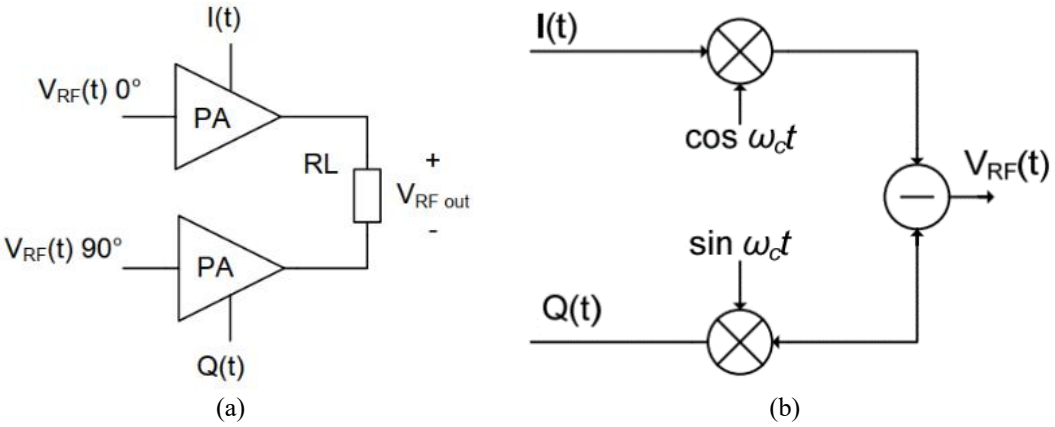


Fig. 1. The general concept of the quadrature power amplifier system: (a) Schematic diagram, (b) RF quadrature modulated signals

The positive and negative supply voltage modulations are VDD=1.2V and VSS=-1.2V, respectively. The load resistance (RL) is placed in the output end that is connected between two nodes ($Vx_I and\ Vx_Q$) of both quadrature modulated signals I(t) and Q(t). These output voltage points should be a sinusoid with constant amplitude of ($\sqrt{{V_{DD}}^2 + {V_{DD}}^2}$) [17].

The quadrature power amplifier system as shown in Fig. 2 is configured using two switching modulating power amplifiers for modulating signals between positive and negative supply voltage (VDD and VSS) respectively. For the positive sign I(t), M1 and M2 are the transmission gate pair that provide the gate-source voltage to feed both transistor pairs (M2 and M3) or (M1 and M3). While for negative sign Q(t), the operation of the transistor pair (M1 and M4) or (M2 and M4) is like the case of positive sign. The output signals of the QPA system are placed at both nodes ($Vx_I and\ Vx_Q$) for the full range of modulated pulse signals like I(t) and Q(t)) respectively. The fundamental tone of the system is operated at the frequency of 5.8GHz that passed using LCR output filter [20].

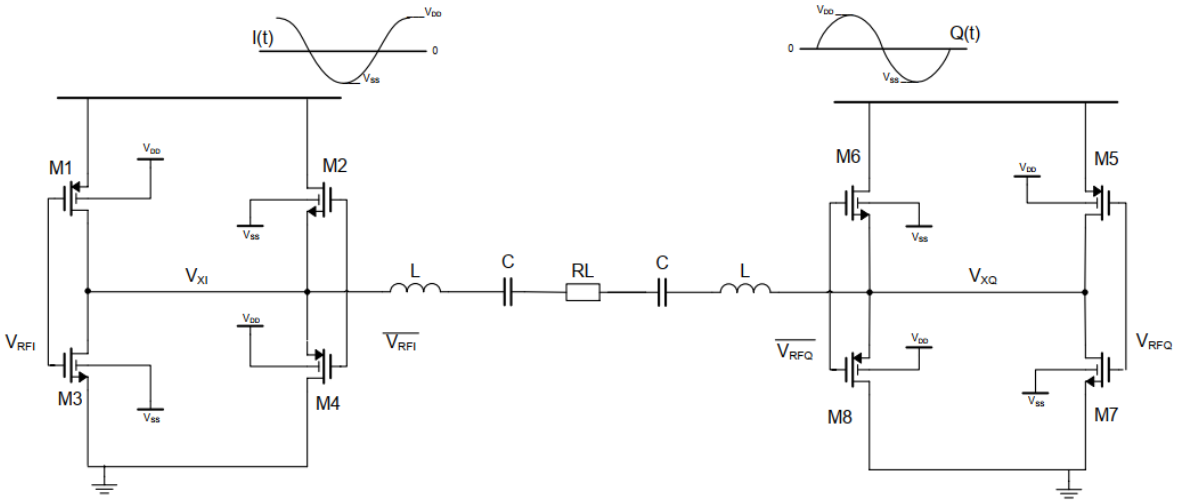


Fig. 2. The quadrature configuration of the power amplifier for both message signals I(t) and Q(t) with both positive and negative supply voltage modulation

3. Transmit RF System Using Quadrature PA

The RF transmitter system consists of quadrature power amplifier (QPAs), driver circuit of QPA, input & output matching circuits, and the transmitted antenna [21]-[22]. The block diagram of this system is shown in Fig. 3. The driver circuit is a hard switching RF pulse signal as a positive or negative depending on the sign of the Quadrature Signals I(t), or Q(t). In the case of positive sign, the RF signal is a pulse signal switching between ground and VDD [23]. Whereas at the opposite sign, the pulse signal switches between VSS and ground (Zero). The construction of the QPAs driver topology to generate these pulse signals is shown on Fig. 4. The QPAs driver circuit consists of an inverter output stage and two sets of switches such as NMOS and PMOS transistors with the channel length of 120 nm process for both positive and negative switching. Both parity bit SI(t) and SQ(t) of both Quadrature signals I(t), and Q(t) respectively drive the two sets of switches positive and negative sign. As a result, the outputs of these switch groups function as power rails for the inverter chain. Then, the duty cycle can be approximately 50% due to having risen and fall times are equal [17].

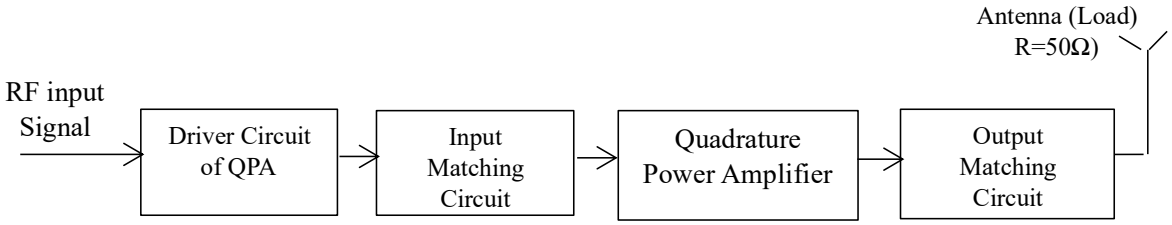


Fig. 3. Block diagram of the transmitted RF signal by using QPA

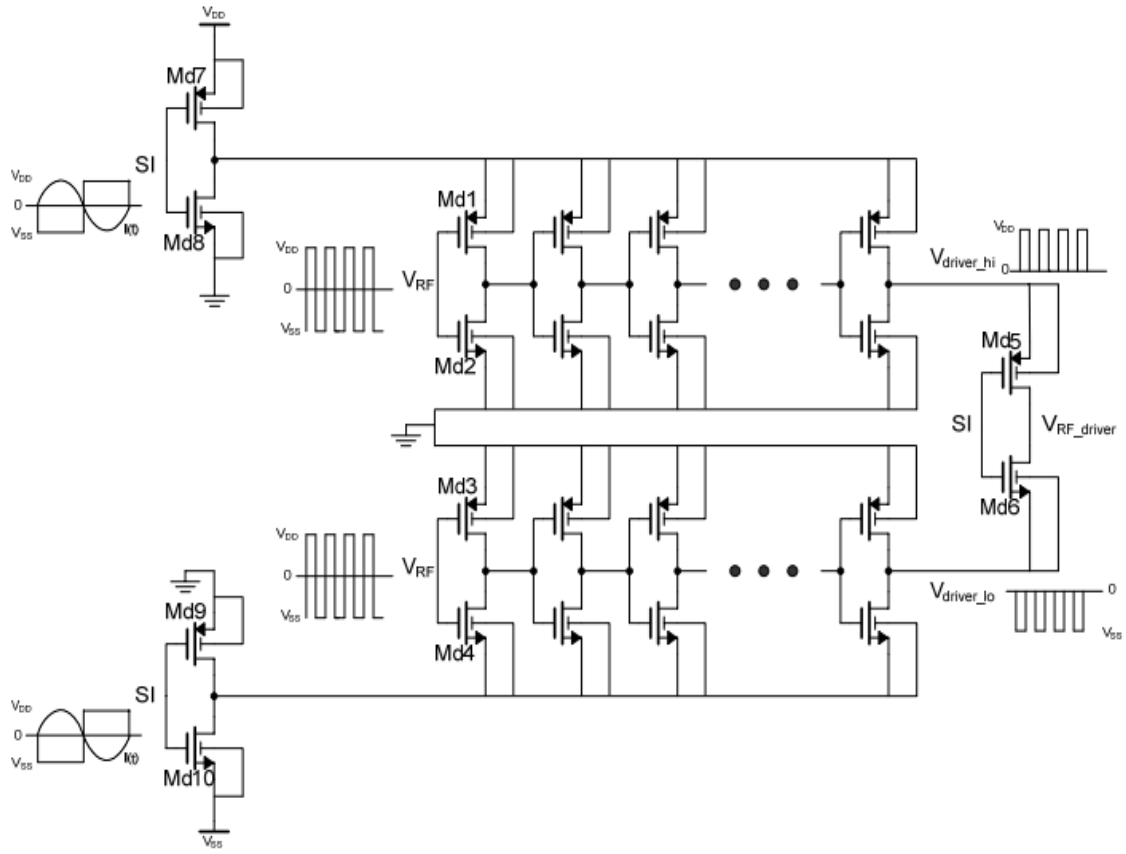


Fig. 4. The driver quadrature PAs architecture

4. Simulation Results and Discussion

The content of the RF transmitter system components such as quadrature PA, driver model of QPA, and matching networks have been designed and performed in an ADS software using 120 nm

CMOS process. The QPAs system operates at the frequency of 5.8GHz and the supply voltage modulated are VDD=1.2 V and VSS=-1.2V. The MOSFET transistors have a 120 nm feature length device (channel length of the gate of all transistors L=120 nm), while the channel widths (W) depend on the fabrication area process. The QPA is used in modern communication systems such as WLAN and 5G that require RF carrier frequency FRF=5.8GHz. Different steps included in the QPA amplifier design like DC biasing simulation, load pull and source pull characteristics, and matching circuit design.

4.1. Biasing and Input Impedance Analysis

The load pull method allows simultaneous measurement of the performance of the DUT by varying the load impedance felt by the DUT. Source extraction also measures the performance of the DUT for different source impedances [21]. The measured results are particularly useful in finding the appropriate load and source impedance for the device to operate at maximum efficiency. For example, load pull is widely used to find the load impedance required to achieve the highest possible efficiency. Source pull is usually needed for a power amplifier, but it is not always necessary. Instead, the inputs are matched in a conjugate fashion. Note that the calculated impedance values are biased. To maximize power added efficiency (PAE), load pull, and source pull were employed in this work. The results of these simulations show that the load and source impedances at 5.8GHz are $(18.252 + j19.015)\ \Omega$ and $(2.929 + j8.349)\ \Omega$ respectively, as shown in Fig. 5.

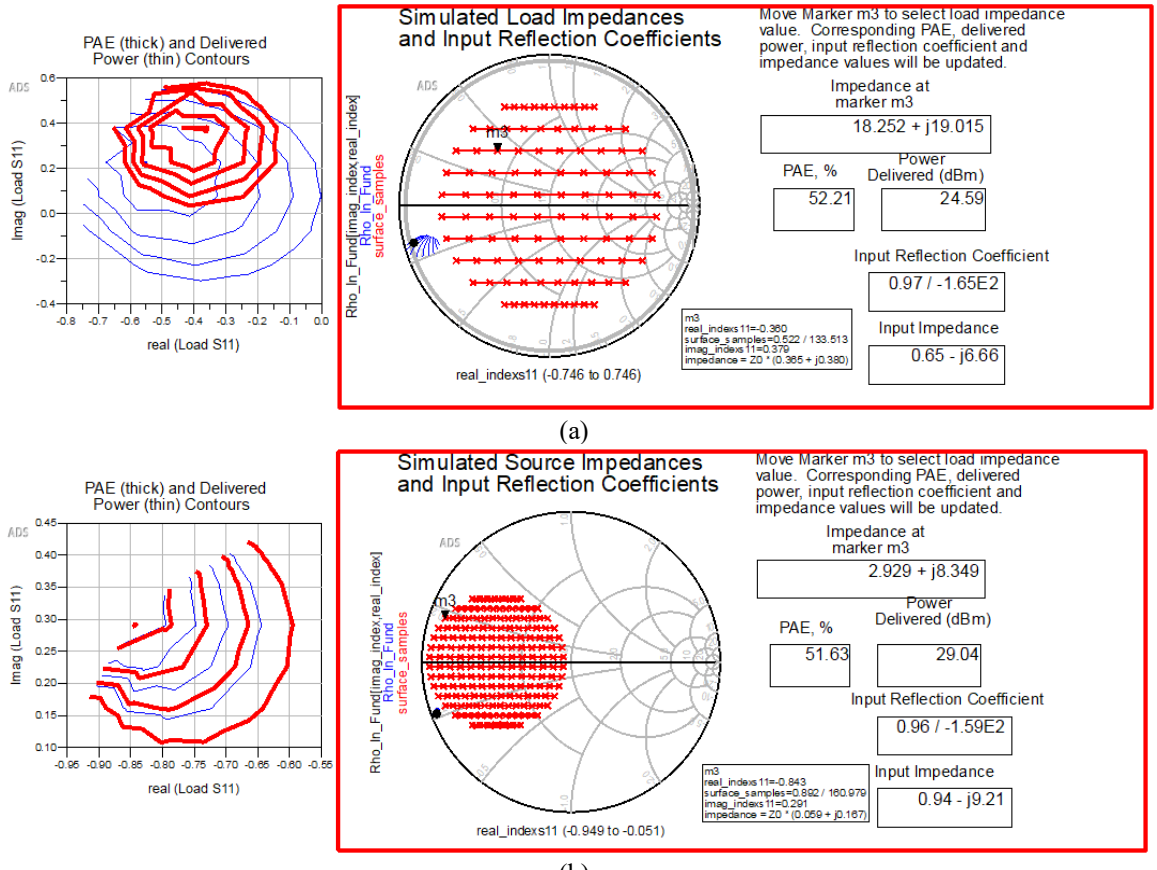


Fig. 5. Analysis to decide input impedance at the maximum efficiency: (a) load pull, (b) source pull

4.2. Quadrature PA and Matching Circuit Simulation Design

The quadrature PA is designed and performed for 120nm CMOS process using ADS simulation software. The four RF hard switching for both positive and negative signs (VRFI, VRFI, VRFQ, and VRFQ) as shown in Fig. 6. The RC-RC filter is driven by the voltage sources at the tunning frequency of FRF=2.4GHz and resulting in two harmonic signals which differ 90° in phase. The general equation of the sinusoidal supply voltage is expressed by (6). Fig. 7 shows the basic architecture design of the

quadrature PAs system. It is seen that the QPA circuit can be divided into two parts $(I(t)_{QPA} and\ Q(t)_{QPA})$ for both supply voltages.

$$V_{RF}(t) = \frac{1}{2\pi\sqrt{RC}} \tag{6}$$

Where the resistor (R) and capacitor (C) are 1kΩ and 66fF, respectively.

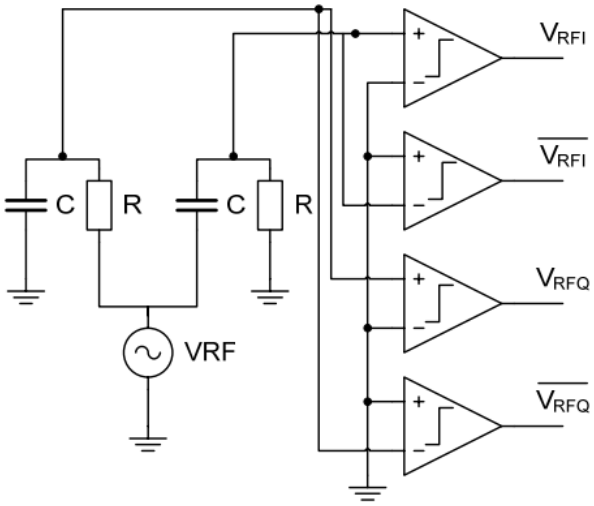


Fig. 6. The driver RF input signals for both message signal signs

4.3. Impedance Matching Circuit Design

For the RF circuit design, the Impedance Matching circuit is an important key to enable RF energy to be injected into the load and achieve highly efficient power transmission. Therefore, the impedance matching network (IMNs) must be adopted. To maximize power transfer between the source and the load, an impedance matching circuit is needed. At the desired operating frequency of 5.8GHz as a case, the impedances of the load and the source (50Ω) are matched such that the impedances are a complex conjugate of each other.

The quadrature PAs circuit design must achieve the closest possible match between the load and the source impedances to conduct highly efficient power transfer. To ensure that the signal is transmitted as efficiently as possible, two factors are needed. Impedance continuity in the circuit, and matching between source and load impedances [22].

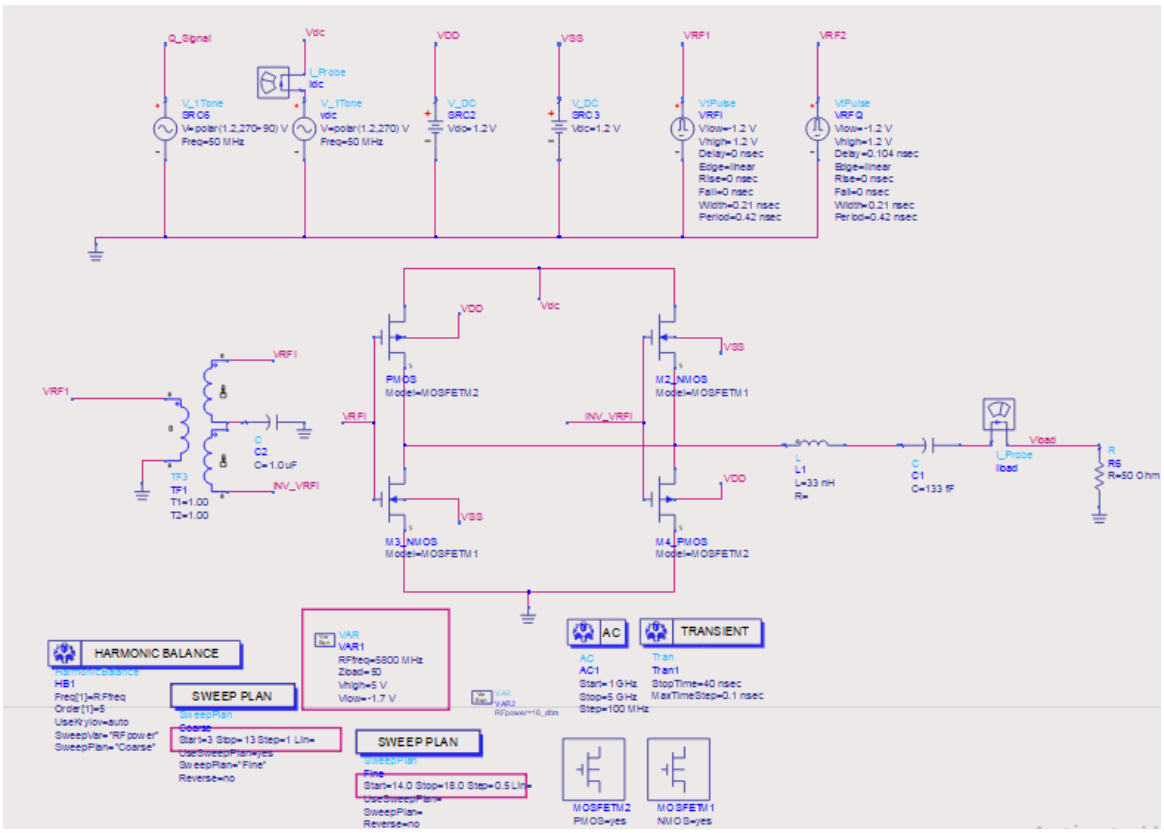
The input and output matched circuits have been designed and constructed at the operating frequency of 5.8GHz to provide the greatest possible design like high dynamic range and power added efficiency (PAE%) improved stable zones of the supply and the load. An L-match, T-match, or π-match are examples of basic discrete element matching networks that can be used to give input and output matching. In this work, L-match is used and implemented using microstrip transmission line (MTLs) technique using a substrate Roger RO-5880 for layout PCB board as reported by Table 1.

Table 1. Roger RO5880 substrate specifications at the frequency of 5.8 GHz

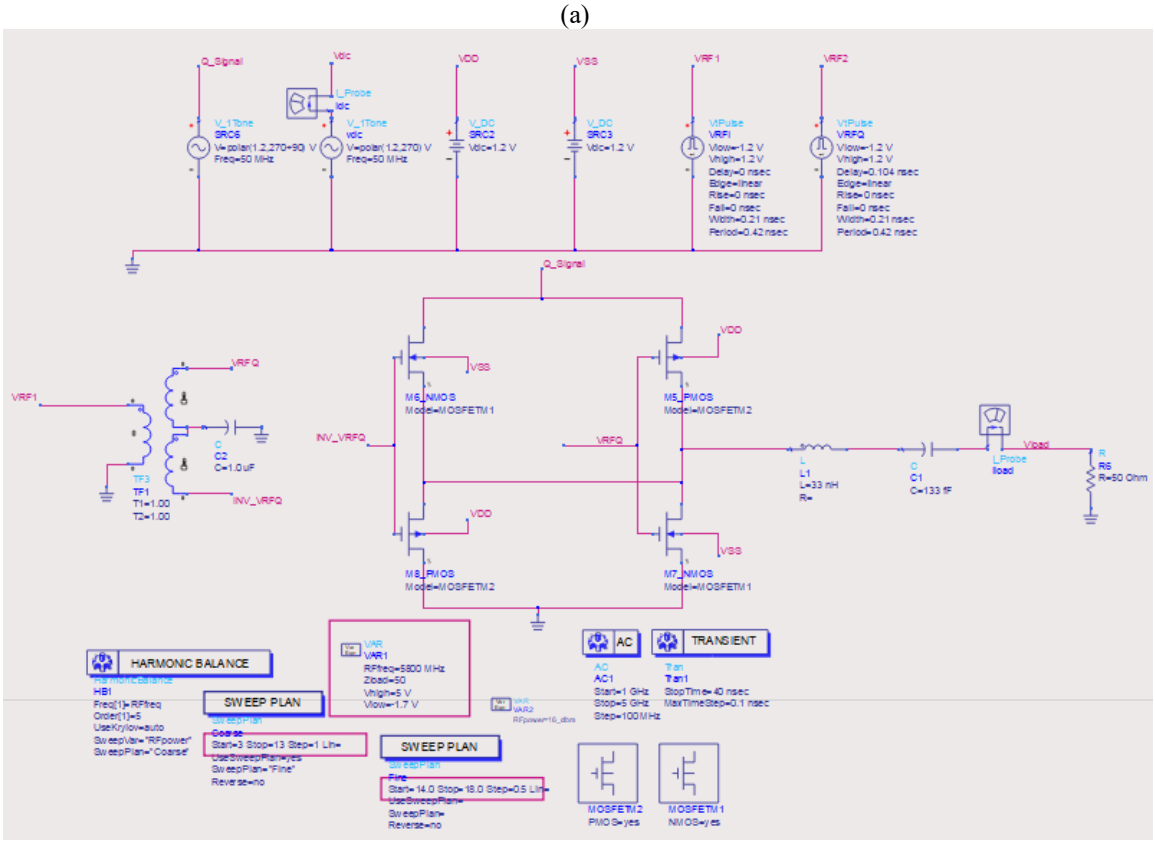
Parameters	Symbol	Value
Dielectric constant (Permittivity)	εr	2.2
Permeability	μr	1
Conductivity	σ	5.8e7 S/m
Thickness of conductor	T	35 μm
Thickness of substrate	H	1.57 mm
Cover height	Hu	3.9e34 mil

This led to the use of source pull and load pull simulations to decide the ideal load and source impedance at a fundamental frequency of 5.8GHz and maximum output power. The pulled-in source

impedance (ZS) was determined to be $(2.929 + j8.349)$ Ω, while the pulled-in load impedance (ZL) was $(18.252 + j19.015)$ Ω.



(a)



(b)

Fig. 7. Single ended CMOS quadrature PAs: (a) I_{QPA} side, (b) Q_{QPA} side

The quality factor of the modulated output network (Q) was chosen to be sufficient to find the matching circuit components at about 10 because a low Q can lead to poor suppression of higher harmonics. A higher (Q factor) can lead to large inductance values reducing power efficiency, and the smallest load is 50 Ω, and the output signal is sinusoidal with no distortions in amplitude and phase. The reflection coefficients (S-parameters S11 and S22) and power gain of these circuits design have been decided at the operating frequency of 5.8GHz and it's explained in Fig. 8.

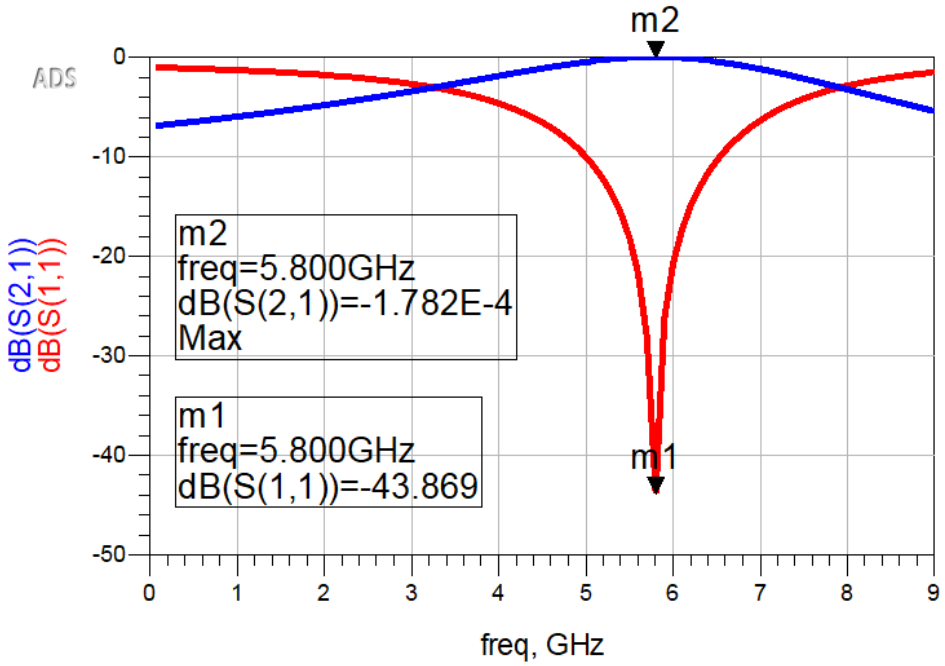


Fig. 8. The simulated reflection coefficient and power gain of matched circuit design

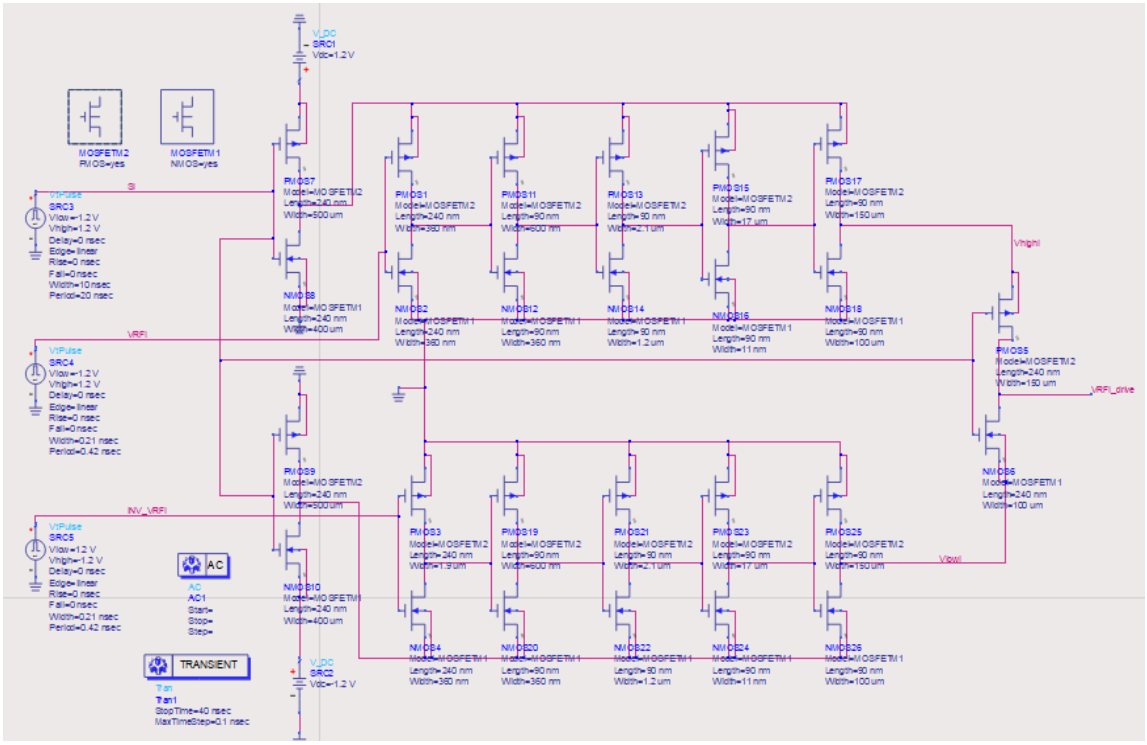
4.4. Envelope and Transient Simulation of QPAs and Driver Circuit

The quadrature PAs is driven by both RF pulse signals positive and negative depending on the sign of the modulated quadrature signals I(t) and Q(t). The supply voltage VDD and VSS have been used in this work of 1.2V and -1.2V, respectively. The two sets of switches in the QPAs driver circuit include NMOS and PMOS transistors with a 120 nm channel length process for both positive and negative switching, as well as an inverter output stage. Due to equal rise and fall times, the duty cycle can be about 50%. The two sets of keys are used by the parity bits SI(t) and SQ(t) of the Quadrature signals I(t) and Q(t), respectively, and have a positive and negative sign, respectively. The output of these sets of switches acts as a supply rail for the inverter series. Fig. 9 shows the topology of the driver circuit design of QPAs that has been constructed using ADS software at the frequency of the message signal is 50 MHz.

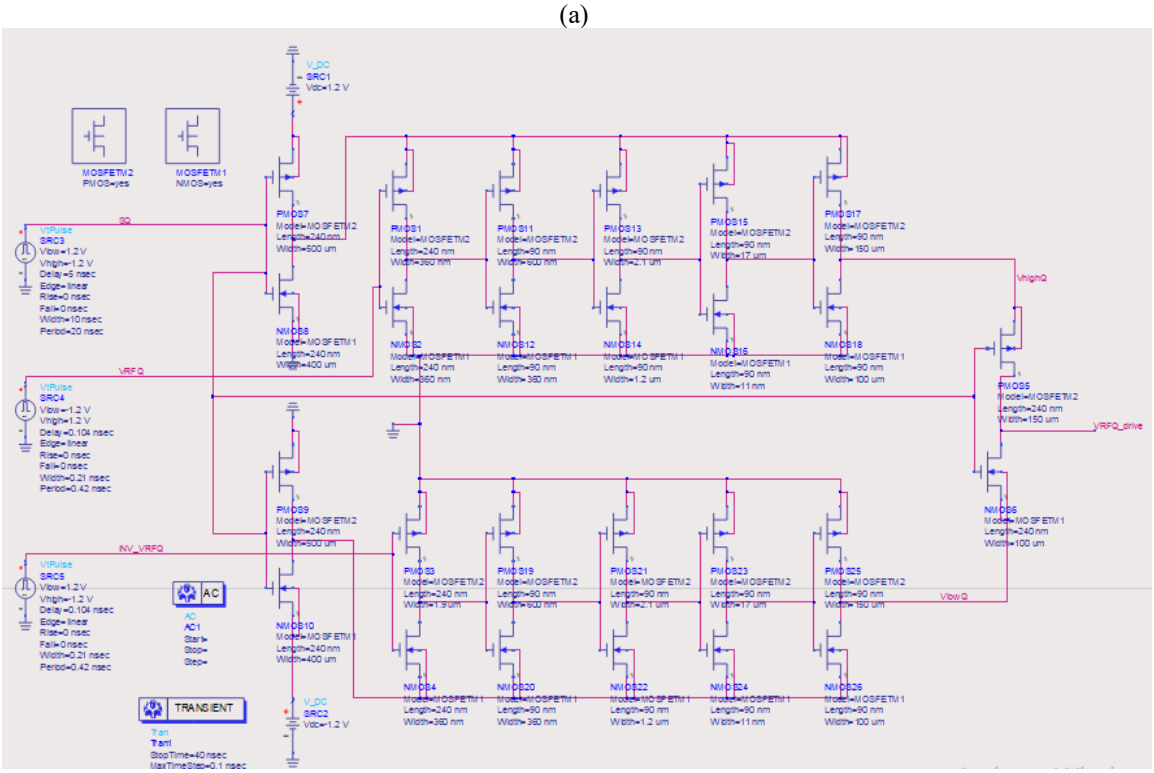
Using transient simulation, the quadrature modulated two signals will be set as sinusoid with difference 90º in the phase and performed at the message signal frequency of FIQ(t) =50MHz. As a result, these two signals generate parity bit signals like SI(t) and SQ(t) that control the operation of the driver QPAs circuit as shown in Fig. 9.

The output QPA driver circuit is a modulated signal with 90º phase shift and ripple occurrence due to different sizes of the transistors used and effect of unbalanced circuit in an uneven output fall and rise times as shown in Fig. 10. The matched circuit has been designed and used to end these ripples. The driver circuits, 90º phase path difference in bridge mode, and matched networks as shown in Fig. 10. Where, the final completely proposed circuit design is shown in Fig. 11 which includes two quadrature Pas.

The simulated QPAs output signal should not be envelope constant as shown in Fig. 12. Therefore, the LCR filter is used for smoothing purposes, and the maximum voltage amplitude is about 0.51 V.



(a)



(b)

Fig. 9. The simulation of the quadrature PAs driver circuits architecture: (a) VRE_I(t) output driver circuit, (b) (a) $VRE_Q(t)$ output driver circuit

4.5. S-Parameters Simulation and Analysis

To obtain S-parameters results such as power added efficiency (PAE%), output power, and linearity, the one-tone harmonic balance (HB) simulation has been performed on the proposed QPA circuit design. HB simulation is a frequency domain analysis technology used to simulate harmonic distortion for evaluating non-linearity of the proposed circuit design at the operating frequency of

5.8GHz. As a result, the HB simulator finds the spectral analysis of both voltage and current. The simulation of the proposed QPA circuit design is investigated using a 1-tone simulator as shown in Fig. 13.

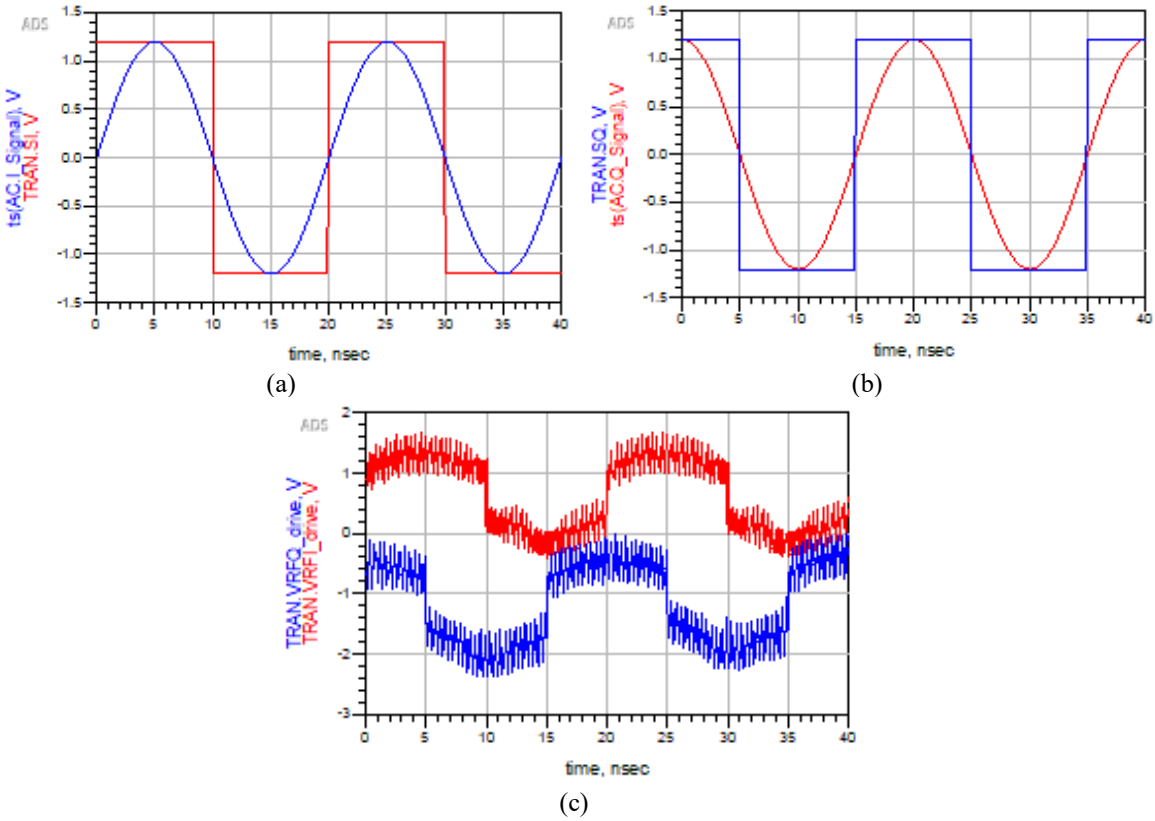


Fig. 10. The simulation output signals of the driver circuits: (a) Message signal I(t) with parity bit SI(t), (b) Message signal Q(t) with parity bit SQ(t), (c) output signal of QPA driver circuits

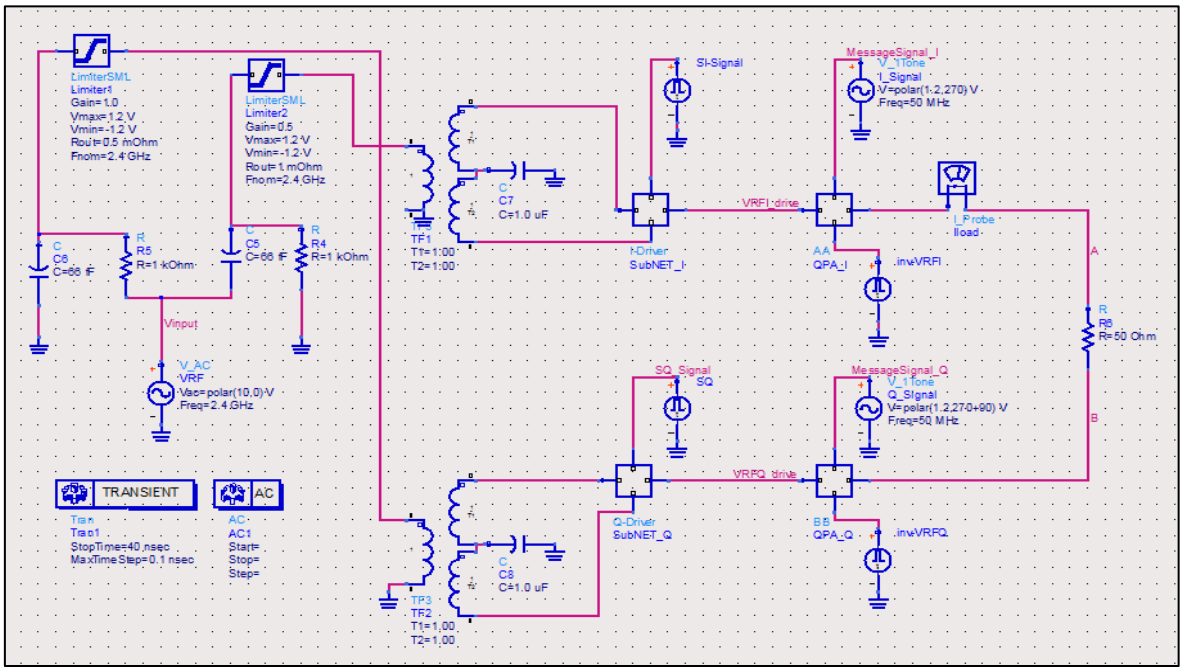


Fig. 11. The simulated of complete circuit design of quadrature power amplifier (QPAs)

The proposed amplifier achieves a good PAE% of about 70% at the maximum output power is 24.35dBm as explained by Fig. 13. The linearity of the proposed QPA was evaluated and performed

at the fundamental frequency of 5.8GHz. The minimum value of amplitude and phase distortion have been obtained in this design is shown on Fig. 14.

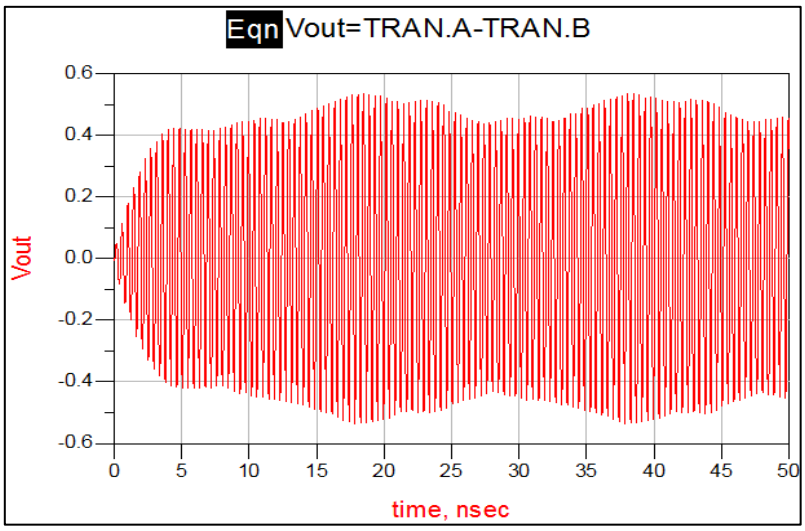


Fig. 12. Output envelope signal of QPA circuit design at the bandwidth of 50MHz with maximum amplitude is 510mV

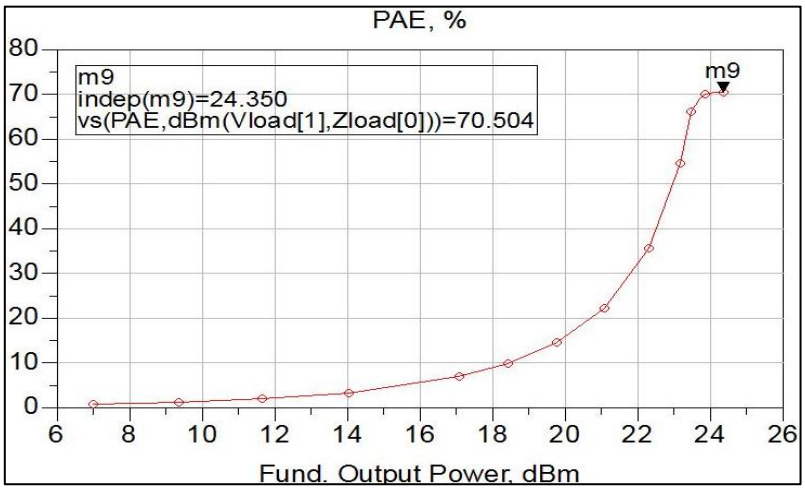
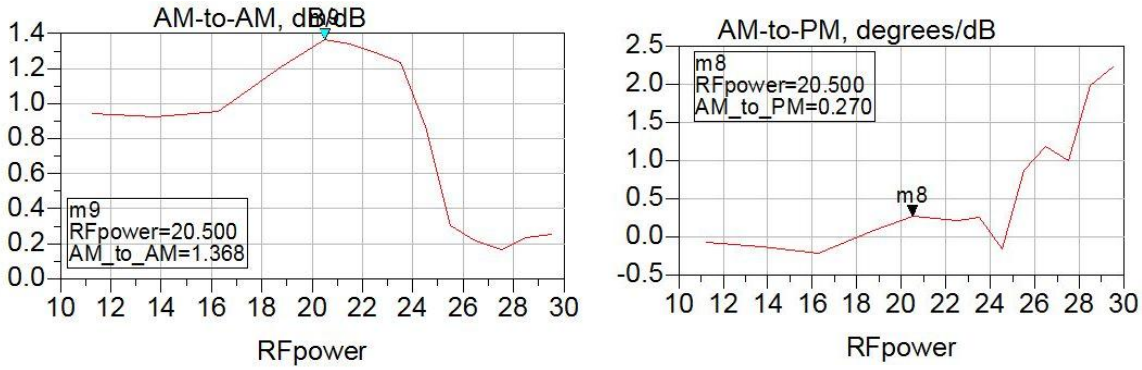


Fig. 13. The simulated PAE% as a function of the output power of the proposed QPA



(a) (b)

Fig. 14. The simulated of :(a) amplitude and (b) phase distortion (AM-to-AM and AM-to-PM) of the proposed QPA amplifier when the input power is greater than 20dBm

Table 2 shows a performance comparison of the proposed Quadrature PAs design with literature review for 5G communication system applications. It saw that the proposed QPA achieves a high

PAE% and gain at the operating frequency of 5.8GHz and low output power is about 24.35dBm. 0.12µm CMOS with envelope elimination and restoration (EER) technologies have been used to investigate quadrature PAs circuit design.

Table 2. Performance comparison of the proposed Quadrature PAs design with literature review

Reported in year	RF Device Process / Topology	Freq. [GHz]	Peak Pdel. [dBm]	PAE [%]	Gain [dB]	B.W [MHz]	Application
[4] 2021	CMOS / Class F DPA	2.45	32	61.8	13	20	Uneven power division
[5] 2016	Class E Hybrid EER	2.4	19	28	6.5	20	WLAN 802.11g
[6] 2023	GaN HEMT / Class J PA	2.4	41	77	13	---	5G systems
[7] 2013	GaN HEMT / Class E PA	2.5	21.46	64	---	---	High power application
[8] 2021	GaAs HEMT / Class F PA	2.4	38.8	65.5	13.8	---	Mobile application
[9] 2021	GaN HEMT / broadband DPA	2.4-3.7	42	61.2	8.1	42.62	5G Mobile communication
[10] 2021	LDMOS / Asymmetric DPA	2.6	46	48	31.7	160	5G systems
[11] 2023	GaN HEMT / DPA	2.6	46.5	58	36	---	Mobile base station
[15] 2022	GaN HEMT / DPA	2-3	44	70	11.2	6	5G systems
This Work	0.12µm CMOS / Quadrature Pas	5.8	43	70	13	50	5G Communication systems

5. Conclusion

This work describes a QuaDRature PA system, 5.8 GHz QPA, based on 0.12 µm CMOS process for 5G communication systems. The design uses Envelope Elimination and Restoration (EER) as a major optimization technique for realizing both high power efficiency and linearity that is necessary to deliver on the requirements of high-speed wireless networks. By using a switch-mode configuration, the QPA effectively amplifies RF signals without the need for any amplitude and phase separation, streamlining the design and improving the performance at a high frequency.

The simulation results show that the simulated QPA design is effective, as the system reaches 70% Power-Added Efficiency (PAE) at 24.35 dBm output using over 20 dBm RF input. The power and thermal management considerations in the mobile and base station applications are reflected strongly in the potential of the results presented here. The QPA efficiently manages two baseband signals modulated in quadrature at a bandwidth of 50 MHz, with an envelope signal with a flat and clean envelope signal with peak amplitude of 510 mV.

Although the design illustrates the effectiveness of CMOS-based EER fill technology in solution of the power-efficient and broadband problems for 5G communication system, there are some limitations that are worth considering. One of these limitations is how the system will perform at varied load conditions which may affect its operational efficiency and linearity in actual, real-world application. Further, several difficulties associated with thermal management at high frequencies and the system's susceptibility to fabrication tolerances, particularly the 0.12 µm CMOS process, should be managed in next work. Moreover, the above claim of "clean signal" generation should be understood in a context that transient ripples, or amplitude/phase distortions seen in earlier results might still condition the functionality of the system and are critical in high bandwidth 5G applications when clean signal is of utmost importance.

As far as the future is concerned, the design for the proposed QPA provides a sound basis for further improvements. The incorporation of digital predistortion (DPD) could increase linearity and multiband operation would increase versatility of its use for different standards of communications. Nevertheless, the introduction of these features entails technical difficulties associated with the requirement for more sophisticated circuitry and greater processing power, which should be considered in future versions. In addition, this system's scalability for integration into other RF front-end components and its compatibility with new wireless systems beyond 5G are still open to study.

Conclusion of this research helps in developing powerful efficient high-performance amplifiers for next generation wireless systems with promising 5G and beyond applications. The proposed design not only shows that CMOS-based QPA systems can be implemented, but it also serves as a platform

for next improvements that may subsequently optimize and integrate RF front end solutions for next generation communication technologies.

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