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Robust Voltage Vector-Controlled Three-Phase SAPF-based BPMVF and SVM for Power Quality Improvement

Bouchaib Essoussi [a,1,*], Ahmed Moutabir [a,2], Bahloul Bensassi [a,3], Abderrahmane Ouchatti [a,4], Yassine Zahraoui [b,5,*], Bouchaib Benazza [c,6]

[a] EIE Laboratory, FSAC, University of Hassan II, Casablanca 5366, Morocco
[b] CCPS Laboratory, ENSAM, University of Hassan II, Casablanca 20670, Morocco
[c] ESE Laboratory, ENSEM, University of Hassan II, Casablanca 8118, Morocco
[1] bouchaib.essoussi1-etu@etu.univh2c.ma; [2] ahmed.moutabir@univh2c.ma; [3] bahloul.bensassi@univh2c.ma;
[4] abderrahmane.ouchatti@univh2c.ma; [5] yassine.zahraoui1-etu@etu.univh2c.ma;
[6] benazzabouchaib@gmail.com
* Corresponding Author

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ABSTRACT

The multiplication of nonlinear loads leads to significant degradation of the energy quality, thus the interconnection network is subject to being polluted by the generation of harmonic components and reactive power, which causes a weakening efficiency, especially for the power factor. In three-phase systems, they can cause imbalances by causing excessive currents at the neutral. This research treats the operation of robust voltage-oriented control (VOC) for a shunt active power filter (SAPF). The main benefit of this technique is to guarantee a decoupled control of the active and reactive input currents, as well as the input reference voltage. To sustain the DC voltage, a robust PI-structure-based antiwindup is inserted to ensure active power control. Besides, a robust phase-locked loop (PLL)-based bandpass multivariable filter (BPMVF) is used to improve the network voltage quality. Furthermore, a space vector modulation (SVM) is designed to replace the conventional one. A sinusoidal network current and unitary power factor are achieved with fewer harmonics. The harmonics have been reduced from 27.98% to 1.55% which respects the IEEE 519-1992 standard. Expanded simulation results obtained from the transient and steady-state have demonstrated the high performance of the suggested control scheme.

1. Introduction

Power electronics is a relatively new and growing field. During the last decades, significant technological development has involved increased use of modern power electronic devices in diverse applications, such as electric machine command, emergency power supplies, dedicated applications electric traction, harmonic compensation, etc. This broad success has mobilized academic scientists on the one hand and industrialists on the other, who have made precious improvements in the technology of semiconductor-based power switches and their controls. These advances have enabled wide distribution at all power levels and in a large number of sectors of activity [1].

However, this multiplication of non-linear loads, especially the rectifiers heavily used at the head

of the power conversion systems, leads to significant degradation of the quality of the energy. Thus the interconnection network is said to be polluted by the generation of harmonic components and reactive power. In three-phase systems, they can cause imbalances by causing immoderate currents in the neutral [2].

To deal with these problems, passive filters are a possible and usual solution. More specifically, passive LC filters are used to reduce harmonic levels, while capacitors alone allow power factor correction. On the other hand, these devices have shown their limits and drawbacks such as fixed compensation, large size, and volume, resonance, and depend on the performances and structures of the network [3].

The significant growth of harmonic pollution has led researchers in power electronics and automation to improve and perfect more efficient and flexible solutions capable of meeting the requirements relating to the excellence of electric energy. This type of device is generally referred to as an active filter (AF) or also called an active power filter (APF) [4], [5].

in the literature, numerous active filter settlements for the depollution of electric networks were discussed. Those that treats today's industrial threats are series or parallel filters and active series-parallel, named unified power-quality conditioners [6], [7]. In the state where the network currents are nonlinear, the SAPF is regarded as the best answer for the mitigation of current ripples in low to medium-power applications. Active filtering is further beneficial when a rapid response is demanded in the existence of potent loads. Additionally, active filters perform as a strong solution for global-goal conditioning as they are capable to offset reactive power as well as load instability [8, 9].

The disadvantages of classical voltage-oriented control (VOC) can be reduced by using space vector modulation (SVM), or so-called VOC-SVM control. The simplicity of the SVM strategy makes it popular. SVMs are based on the inverter space vector representation. In this method, the SVM block ensures a constant switching frequency. The VOC-SVM technique calculates the voltage inverter states, in order to achieve the following needs: decreased power harmonics and constant switching frequency [10], [11].

In order to comply with the binding electrical quality standards enforced on industrial suppliers and consumers and in goal to curb the rise in disturbance problems on electrical networks, active filters have to adjust and fulfill these demands and therefore enhance their topologies and command methods [12]. To this end, many research works keep to be published on the SAPF, regarding three principal zones. The first is the estimation of the current to be compensated, the second is to assess other possible structures, and the third treats the command techniques that deliver the command signals of the power switches. In [13], a 3-leg split-capacitor SAPF (TLSC) is designed to provide reactive and harmonic compensation as well as DC-link bus voltage control by means of H∞ controllers. The authors in [14] present a technique of command for the SAPF that measures currents only. A redesigned technique is used to abstract negative and positive string components. In [15], the authors proposed a voltage sensor-less command technique for a shunt APF that demands only current measurements. By analyzing the negative sequence components of these currents, reference currents are defined for the inverter in the shunt APF.

This paper intends to improve the SAPF classical voltage-oriented control by:

- Removing the classical PWM and replacing it with a robust one-based SVM.
- Inserting a robust PLL structure based on BPMVF.
- Replacing the classical PI controllers with robust structure-based antiwindup.

This research is arranged as: Section 1 presents an introduction to the subject with a literature review background. Section 2 depicts the suggested PLL-based BPMVF and the DC-link voltage-based antiwindup. Section 3 demonstrates the basics of VOC for SAPF. Section 4 details the numerical SVM algorithm. Section 5 gives the simulation protocol and a discussion of the results. At last, section 6

presents a conclusion of the paper.

2. Robust PLL-based BPMVF and DC-link-based Antiwindup

2.1. Conventional PLL

The PLL is a clef unit in recent command methods. It is utilized as a manner to recover frequency and phase information, especially the angular position (θ_s) [16]. The fundamental PLL form is depicted in Fig. 1, containing a phase spotter, a loop-filter which is normally a PI regulator, and a voltage-commanded oscillator.

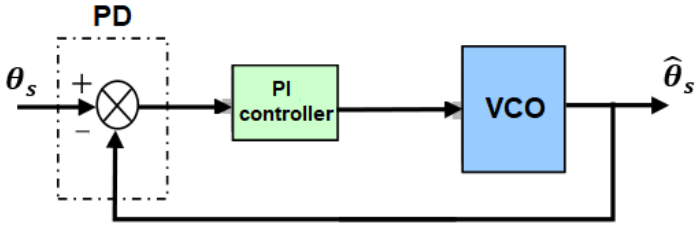


Fig. 1. Conventional PLL structure

Many PLL structures have been detailed, Fig. 2 shows the architecture of the conventional PLL. The phase to neutral network voltages are defined as:

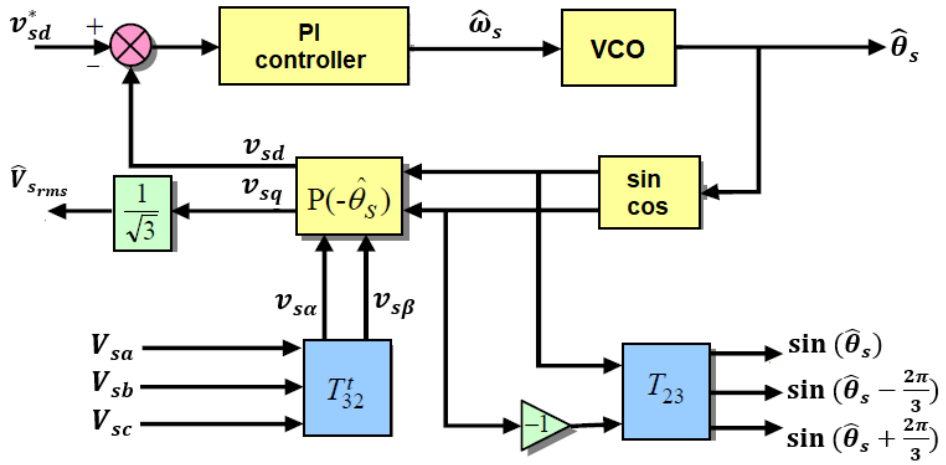


Fig. 2. Architecture of conventional PLL

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} \sqrt{2}V_{s_{rms}} cos(\theta_s) \\ \sqrt{2}V_{s_{rms}} cos(\theta_s - \frac{2\pi}{3}) \\ \sqrt{2}V_{s_{rms}} cos(\theta_s + \frac{2\pi}{3}) \end{bmatrix} \tag{1}$$

$V_{s_{rms}}$, θ_s, and ω_s are the root-mean square network-voltage, the angle of the phase, and the pulsation of the voltage. The transformation that permits to move to the corresponding 2-phase coordinates is:

$$\begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} \sqrt{3}V_{s_{rms}} sin(\theta_s) \\ -\sqrt{3}V_{s_{rms}} cos(\theta_s) \end{bmatrix} \tag{2}$$

The synchronously d-q rotating frame quantities can be obtained by passing through the Park conversion:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}_s) & sin(\hat{\theta}_s) \\ -sin(\hat{\theta}_s) & cos(\hat{\theta}_s) \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{3}$$

When $\hat{\theta}_s - \theta_s$ is small-scale, v_{qs} in (3) would be:

$$v_{qs} = \sqrt{3} V_{s_{rms}} (\hat{\theta}_s - \theta_s) \tag{4}$$

The PLL will be triggered when $\hat{\theta}_s$ is the same as θ_s, hence v_{sq}=0. Based on Fig. 1, the estimated pulsation is (5):

$$\hat{\omega}_s = FLF(s)(\theta_s - \hat{\theta}_s) \tag{5}$$

FLF(s) is the filter loop, it is expressed by (6):

$$FLF(s) = K_{pp} + \frac{K_{ip}}{s} = K_{pp}(\frac{1 + \tau_{ip} s}{\tau_{ip} s}) \tag{6}$$

where τ_{ip}=$\frac{K_{pp}}{K_{ip}}$, K_{pp}, and K_{ip} are the antiwindup regulator gains. Hereafter, $\hat{\theta}_s$ at the VCO output will be (7):

$$\hat{\theta}_s = \frac{1}{s} \hat{\omega}_s \tag{7}$$

In the aim to find the PID regulator parameters, the bloc diagram of Fig. 2 may be simplified to be approximate to that of Fig. 1 as it is shown on the synoptic of Fig. 3:

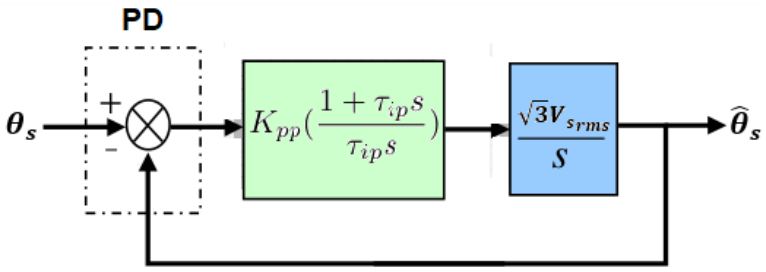


Fig. 3. Classic PLL

$$\frac{\hat{\theta}_s}{\theta_s} = \frac{\sqrt{3} V_{s_{rms}} K_{pp} (\frac{1+\tau_{ip}}{\tau_{ip} s}) \frac{1}{s}}{1 + \sqrt{3} V_{s_{rms}} K_{pp} (\frac{1+\tau_{ip}}{\tau_{ip} s}) \frac{1}{s}} \tag{8}$$

This function could be identified as:

$$F(s) = \frac{\hat{\theta}_s}{\theta_s} = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{9}$$

The filter-loop parameters are then given as:

$$\begin{cases} K_{pp} = \frac{2\zeta\omega_n}{\sqrt{3} V_{s_{rms}}} \\ \tau_{ip} = \frac{2\zeta}{\omega_n} \end{cases} \tag{10}$$

In the purpose to have a good settlement between performance and stability, the next parameters are engaged: ζ=0.7, K_{pp}=1.05, K_{ip}=237.5, and τ_{ip}=$5.10^{-3}s$.

2.2. The Suggested BPMVF PLL

There are numerous techniques to surmount the raised issues, we highlight PLL based on RST controllers [17], fuzzy logic [18], neural networks [19], or Adaline networks [20]. All these techniques fulfill a settlement between good dynamics and network voltage disturbances insensitivity.

The method presented in this research relies in the use of multivariable filters guaranteeing the decoupling between the dynamic performance and the sensitivity to load variation. To demonstrate the efficacy of the proposed PLL, we will first survey the filter operation and hence the new PLL behavior by establishing a comparison with the conventional PLL. Afterward, the new PLL robustness can be validated. Whence, the expression of the structural form of the BPMVF that is inserted in the PLL is [21]:

$$\begin{cases} \hat{v}_{s\alpha} = \frac{k_c}{s}[v_{s\alpha} - \hat{v}_{s\alpha}] - \frac{\omega_c}{s}\hat{v}_{s\beta} \\ \hat{v}_{s\beta} = \frac{k_c}{s}[v_{s\beta} - \hat{v}_{s\beta}] - \frac{\omega_c}{s}\hat{v}_{s\alpha} \end{cases} \tag{11}$$

k_c and ω_c are adjusting gains. The bloc diagram of the new structure is explained in Fig. 4.

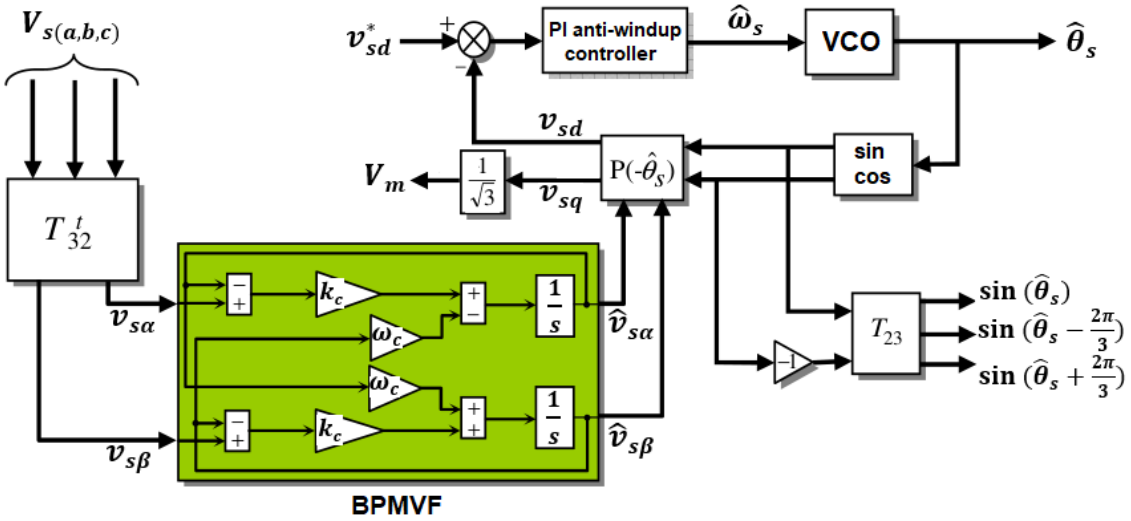


Fig. 4. BPMVF for robust PLL structure

2.3. DC Regulator-based Antiwindup

In this part, the DC link regulator is synthesized in such a way that the voltage gap is the smallest. The suggested regulator consists of a PI antiwindup. Let's define the DC-link voltage structure:

$$i_{dc} = C_{dc}\frac{dV_{dc}}{dt} \tag{12}$$

Coupling filters and the power losses of the inverter switches are dropped, and the power equilibrium among AC and DC sides is expressed by exploiting the instantaneous power theory:

$$V_{dc}^{*} i_{dc} = \frac{3}{2}(v_{sd} i_{sd} + v_{sq} i_{sq}) \tag{13}$$

where v_{sdq} and i_{sdq} are the network-voltage and current. Substituting (12) into (13) gives:

$$V_{dc}^{*}(C_{dc}\frac{dV_{dc}}{dt}) = \frac{3}{2}(v_{sd} i_{sd} + v_{sq} i_{sq}) \tag{14}$$

Supposing that the source-voltages are balanced then v_{sd} equals 0 while the synchronization is produced by a PLL. Consequently, (14) will be:

$$\frac{dV_{dc}}{dt} = \frac{3}{2}\frac{v_{sd}}{V_{sd}^{*}C_{dc}}i_{sd} \tag{15}$$

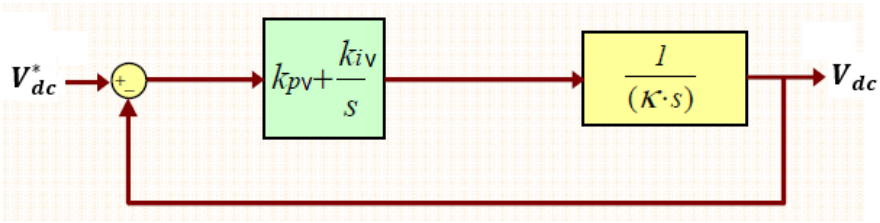
We know that v_{sd}=$\sqrt{2}V_{s_{rms}}$, hence:

$$\frac{V_{dc}(s)}{i_{sd}(s)} = \frac{3}{\sqrt{2}}\frac{V_{s_{rms}}}{V_{dc}^{*}C_{dc}s} \tag{16}$$

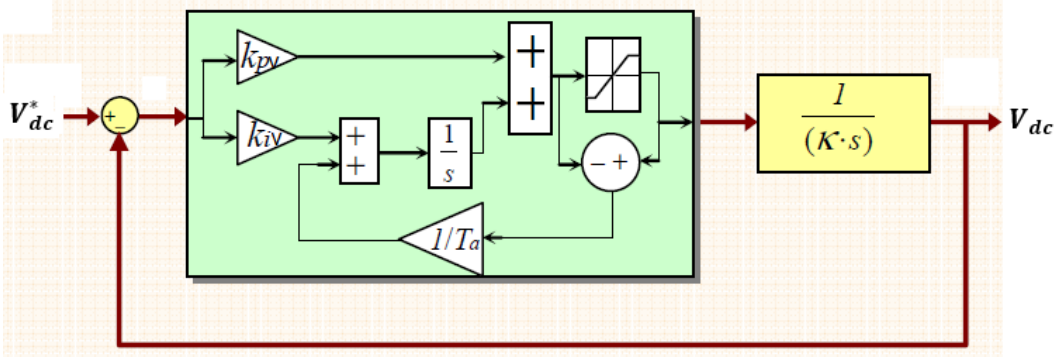
Let's define K=$\frac{i_{sd}(s)}{V_{dc}(s)}$, from (16):

$$K = \frac{\sqrt{2}}{3}\frac{C_{dc}V_{dc}^{*}}{V_{s_{rms}}} \tag{17}$$

To maintain the DC-link at the wished interval, a PI-based antiwindup is utilized in compliance with the Fig. 5.



(a) Conventional PI



(b) PI-based antiwindup

Fig. 5. Suggested link voltage regulator

With the aim to reduce the DC-link fluctuations and balance for system losses, a PI regulator described by $G_{V_{dc}}$ is chosen [22], [23].

$$G_{V_{dc}} = \frac{K_{pv}s + K_{iv}}{Ks^2 + K_{pv}s + K_{iv}} = \frac{\frac{K_{pv}}{K}(s + \frac{K_{iv}}{K_{pv}})}{s^2 + \frac{K_{pv}}{K}s + \frac{K_{iv}}{K}} \tag{18}$$

K_{pv} and K_{iv} are the antiwindup adjusting gains. Hence:

$$s^2 + 2\zeta\omega_n + \omega_n^2 = s^2 + (\frac{K_{pv}}{K})s + \frac{K_{iv}}{K} \tag{19}$$

By identification of (19):

$$\begin{cases} K_{pv} = 2\zeta\omega_n K \\ K_{iv} = K\omega_n^2 \end{cases} \tag{20}$$

It is important to keep in mind that the antiwindup of the integral term, which results from saturation, causes the control to operate in an open-loop during a transient with a significant magnitude and, as a result, causes excessive integration of the error. An antiwindup structure is used to address this issue. The DC-link error is zero as long as the regulator output isn't saturated. When saturation happens, there is a counter-reaction toward the integrator's input, amplified by a gain $\frac{1}{T_a}$ (T_a=10^{-3}) [24].

The following tuning gains are kept in order to achieve the ideal balance between dynamic performance and stability: ζ=0.707, K_{pv}=0.118, and K_{iv}=6.41. Fig. 6 demonstrates the response of the V_{dc} closed-loop to a step reference, and hence the high-performance of the suggested DC-bus voltage regulator.

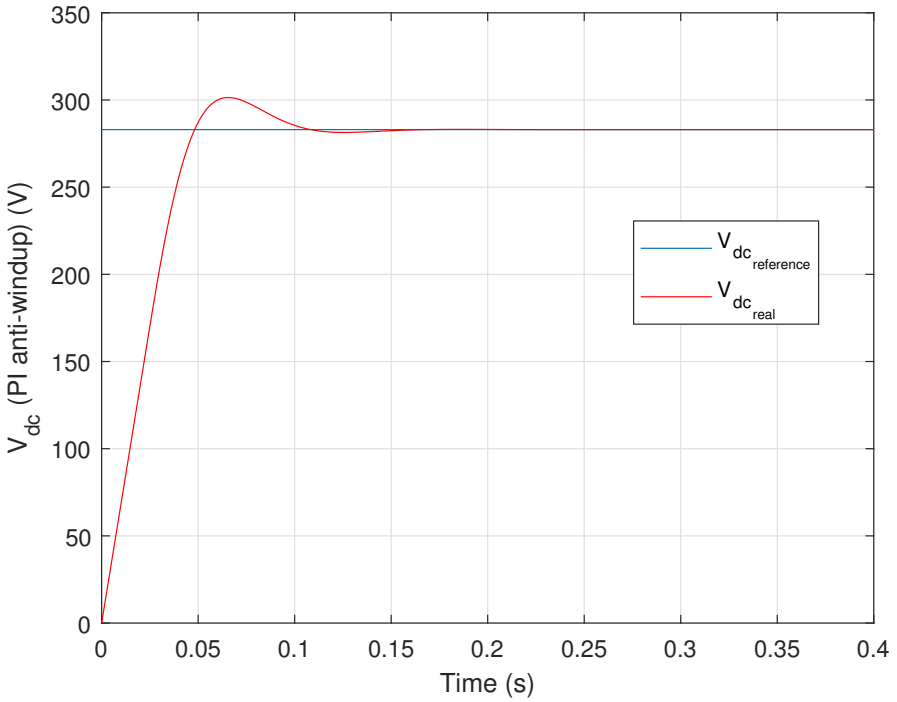


Fig. 6. V_{dc} closed-loop response

3. VOC Principle

Identically as in field-oriented control (FOC) of an induction motor [25], based on the coordinate transformation between α-β and d-q reference frames, VOC for line-side PWM rectifier is used. This control law guarantees quick transient response and high static operation by means of internal current regulation loops. As a result, the ultimate configuration and operation of the system mainly rely on the excellence of the applied current command [26].

The simplest choice is hysteresis current command that supplies a quick dynamics, good precision, no DC-offset, and high effectiveness. But, the crucial issue of hysteresis command is that its normal switching frequency changes with the load variation, which yields the switching motif unequal and random, so, ensuing in extra stress on switches and troubles of LC input filter. Thus, many

strategies are pointed out in the literature to enhance the operation of the current command [27]. Between presented controllers, the broadly utilized scheme for high-operation current command is the d-q synchronous regulator, where the currents being controller are DC-quantities that eliminate steady-state gap [28]. The synchronous reference's voltage equations are:

$$u_{ld} = R_s i_{ld} + L\frac{di_{ld}}{dt} + u_{sd} - \omega L i_{lq} \tag{21}$$

$$u_{lq} = R_s i_{lq} + L\frac{di_{lq}}{dt} + u_{sq} + \omega L i_{ld} \tag{22}$$

u_{ld}, u_{lq}, i_{ld}, and i_{lq} are the load d-q voltages and currents respectively. u_{sd} and u_{sq} are the source (network) voltages.

The q-current reference i_{sq}^* is forced to 0 in all conditions for unitary power factor whereas the d-current reference i_{sd}^* is set by the DC-bus regulator and commands the active power flowing. For $R_s \approx 0$, (21) and (22) could be summarized to:

$$u_{ld} = L\frac{di_{ld}}{dt} + u_{sd} - \omega L i_{lq} \tag{23}$$

$$u_{lq} = L\frac{di_{lq}}{dt} + u_{sq} + \omega L i_{ld} \tag{24}$$

Supposing that the i_{sq}^* component is well controlled to 0, the following equations still true:

$$u_{ld} = L\frac{di_{ld}}{dt} + u_{sd} \tag{25}$$

$$u_{lq} = L\frac{di_{lq}}{dt} + u_{sq} \tag{26}$$

As the current regulator, the PI-type could be utilized. But, the PI current regulator has no satisfying operation, particularly, for the coupled system depicted by (25) and (26). Thus for high-operation application with accurate current tracking at dynamic state, the decoupled regulator diagram for the PWM rectifier is highlighted in Fig. 7:

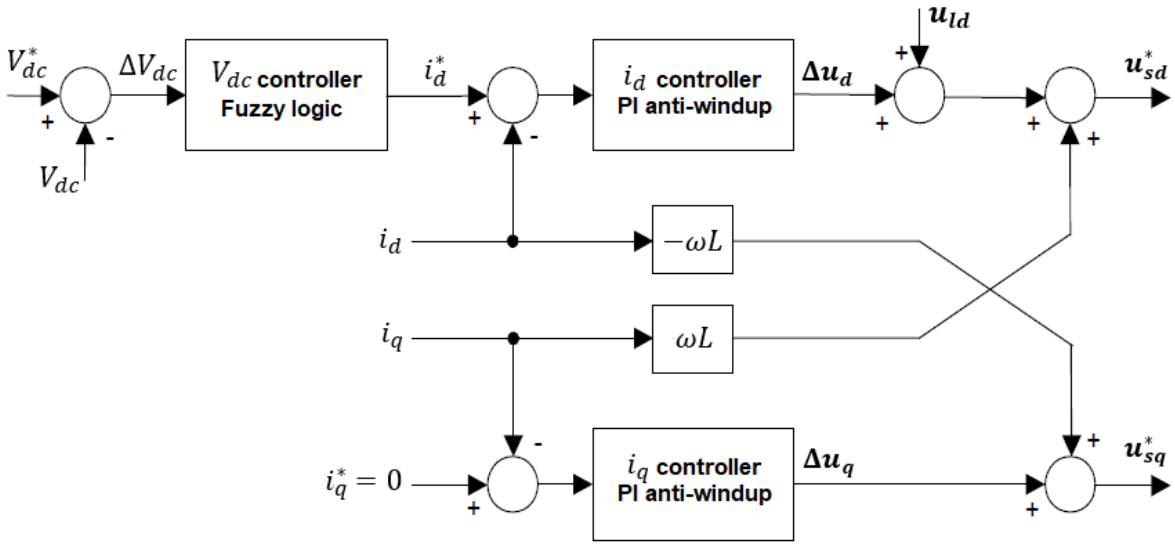


Fig. 7. Decoupled current control of voltage-oriented control

Hence:

$$u_{ld} = \omega L i_{lq} + u_{sd} + \Delta u_{sd} \tag{27}$$

$$u_{lq} = -\omega L i_{ld} + \Delta u_{sq} \tag{28}$$

where Δ is the output signal of the current regulators:

$$\Delta u_{sd} = K_{pi}(i_{sd}^{*} - i_{sd}) + K_{ii} \int (i_{sd}^{*} - i_{sd})dt \tag{29}$$

$$\Delta u_{sq} = K_{pi}(i_{sq}^{*} - i_{sq}) + K_{ii} \int (i_{sq}^{*} - i_{sq})dt \tag{30}$$

The output signals from PI regulators after d-q — α-β transformation are utilized for switching signals generated by the SVM modulator.

4. Space Vector Modulation Algorithm

SVM is separated from PWM. It depends on the inverter output spatial vector representation. There are no distinct modulation for each phase. The reference voltages are generated by the spatial voltage vector. The SVM goal is the prediction of the inverter voltage vector by the projection of the reference vector V_s^* between two adjacent vectors corresponding to 2 non-zero switching states [29], [30].

Vector modulation uses a numerical algorithm to get an inverter switch command sequence to give an output voltage vector that comes as close as possible to the reference voltage. For the 2-level inverter, the switching vector diagram creates a hexagon divided into 6 sectors, each of which is offset by the other by 60°, as depicted in Fig. 8.

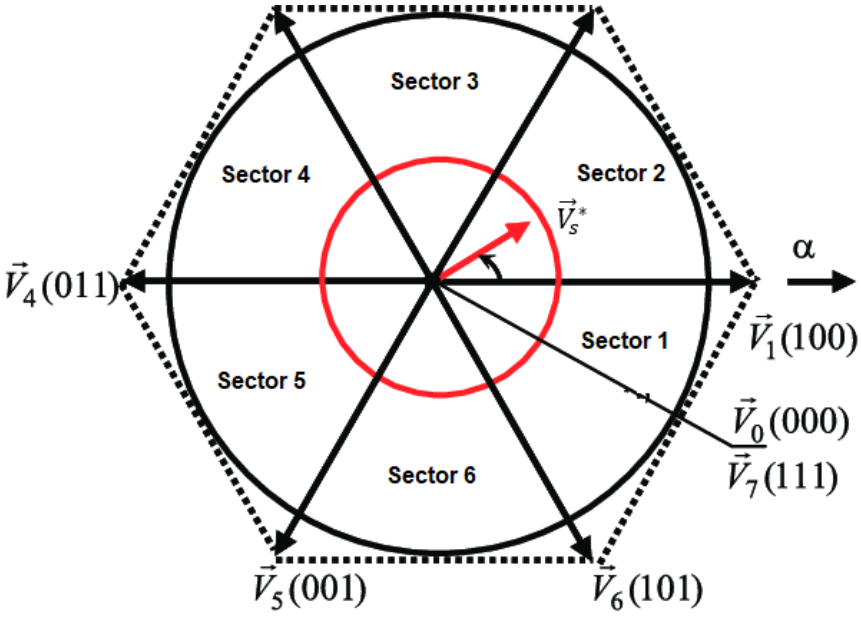


Fig. 8. Space vector distribution of the voltage vector

The application time of each vector could be achieved by vector computations and the remainder of the period will be filled by applying the V_0 vector. When sector 1 is occupied by the reference voltage Fig. 9, it is then synthesized utilizing the vectors V_1, V_0 and V_2. The second principle of the volt for sector 1 can be formulated by:

$$V_s^* t_z = t_1 V_1 + t_2 V_2 + t_0 V_0 \tag{31}$$

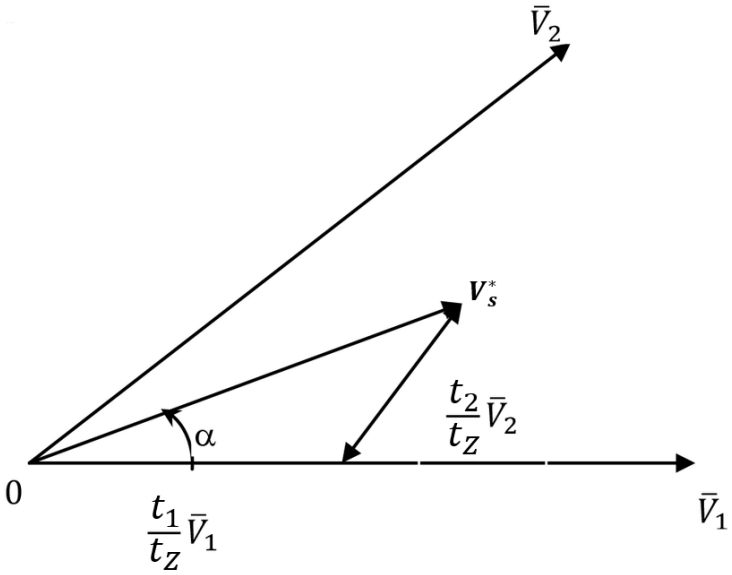


Fig. 9. Reference vector as an association of adjacent vectors

$$t_z = t_0 + t_1 + t_2 \tag{32}$$

The voltage vectors V_1, V_2, and V_0 are applied at times t_1, t_2, and t_0. The sampling time is t_z. The resolution of the times t_2 and t_1 is achieved by simple projections:

$$t_1 = \frac{t_z}{2V_{dc}}(\sqrt{6}V_{s\beta}^* - \sqrt{2}V_{s\alpha}^*) \tag{33}$$

$$t_2 = \sqrt{2}\frac{t_z}{V_{dc}}V_{s\alpha}^* \tag{34}$$

V_{dc} is the DC voltage. The calculus of the working cycles is done as:

$$t_{a_{ON}} = \frac{t_z - t_2 - t_1}{2} \tag{35}$$

$$t_{b_{ON}} = t_1 + t_{a_{ON}} \tag{36}$$

$$t_{c_{ON}} = t_2 + t_{b_{ON}} \tag{37}$$

Table 1 summarizes each sector switching (output) times and Fig. 10 illustrates the switching times of the first sector:

Table 1. Each sector switching times

$\Delta\phi_s$	1	2	3	4	5	6
S_a	$t_{b_{ON}}$	$t_{a_{ON}}$	$t_{a_{ON}}$	$t_{c_{ON}}$	$t_{b_{ON}}$	$t_{c_{ON}}$
S_b	$t_{a_{ON}}$	$t_{c_{ON}}$	$t_{b_{ON}}$	$t_{b_{ON}}$	$t_{c_{ON}}$	$t_{a_{ON}}$
S_c	$t_{c_{ON}}$	$t_{b_{ON}}$	$t_{c_{ON}}$	$t_{a_{ON}}$	$t_{a_{ON}}$	$t_{b_{ON}}$

5. Simulation Results and Discussion

5.1. System's Presentation

A full model is designed with the parameters listed in Table 2, the goal is to analyze the operation of the suggested VOC-SVM applied to the SAPF.

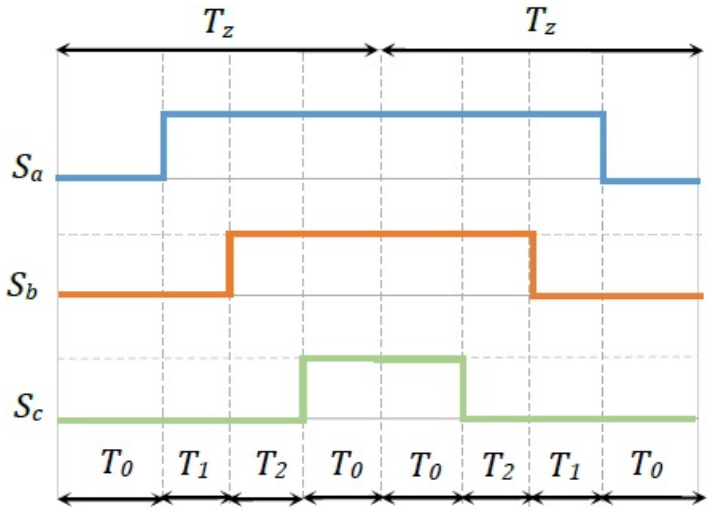


Fig. 10. Sector 1 switching time

Table 2. Source, nonlinear load, and SAPF parameters

Source	RMS voltage	220 V
	Frequency	50 Hz
	Internal resistor	0.1 Ω
	Internal inductor	0.1 mH
Nonlinear load	Load resistor	30 Ω
	Load inductor	1 mH
	Rectifier resistor	0.01 Ω
	Rectifier inductor	0.566 mH
SAPF	Bus capacitor	1100 μF
	Filter inductor	1 mH
	Reference voltage	600 V
Simulation environment	Sampling time	1 μs
	Step type	Fixed step
	Resolution method	Euler (ode1)

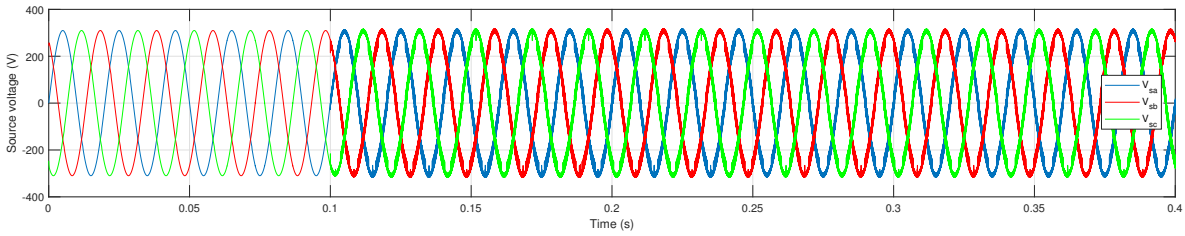
First, Fourier analysis of current waveforms and a comparison of their THDs will be used to examine the effectiveness of filtering. The command stability and robustness are then evaluated in the closure of SAPF on the source and nonlinear load. At t=0.1s, the filter is set up, and a load resistor variation from 30Ω to 15Ω is applied. The DC-link capacitor receives a 500V initial charge.

The signals arranged in Fig. 11 are the source voltage, the PLL voltage, the source current, the load current, the filter current, and the DC-bus voltage. The signals arranged in Fig. 12 are the SVM switching states, the inverter switching states, and the network voltage and current. Fig. 13 shows the source's current THD before and after filtering.

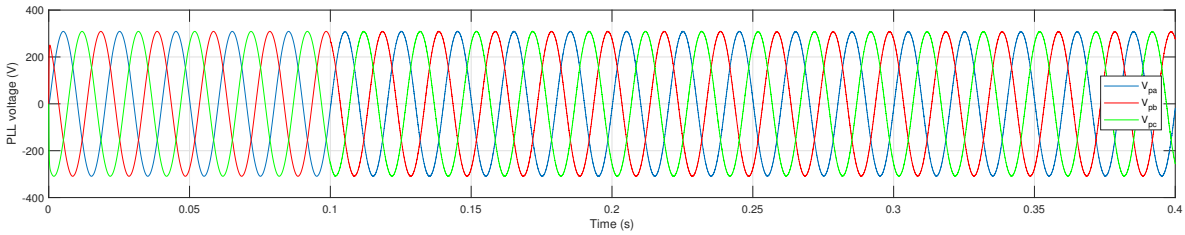
5.2. Results Analysis

5.2.1 PLL Robustness

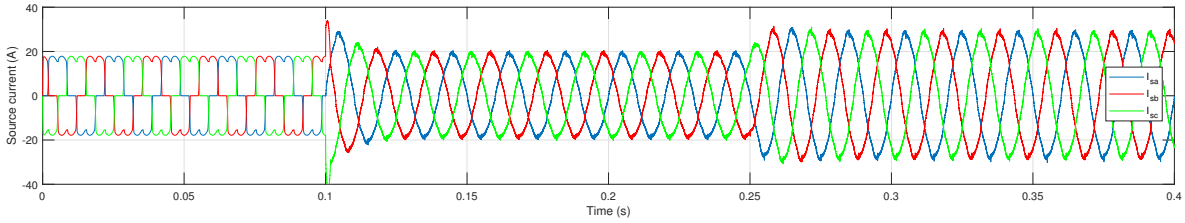
Fig. 11(a) shows the network voltage before and after the filter closure, the voltage waveform becomes chopped after the filter closure. Fig. 11(b) shows the PLL voltage before and after the filter closure, there is no change in the voltage waveform which indicates the robustness of the suggested PLL-based BPMVF and antiwindup.



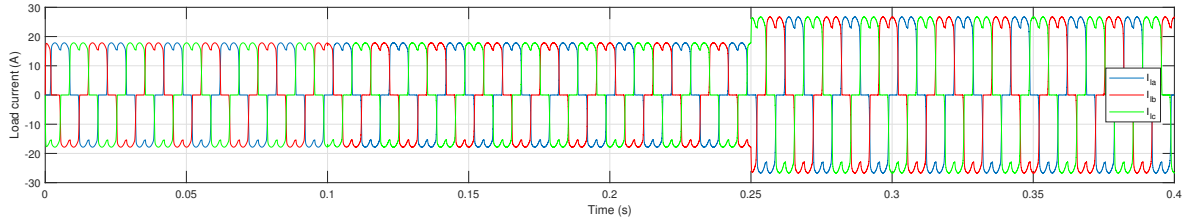
(a) Source voltage: proposed VOC-SVM



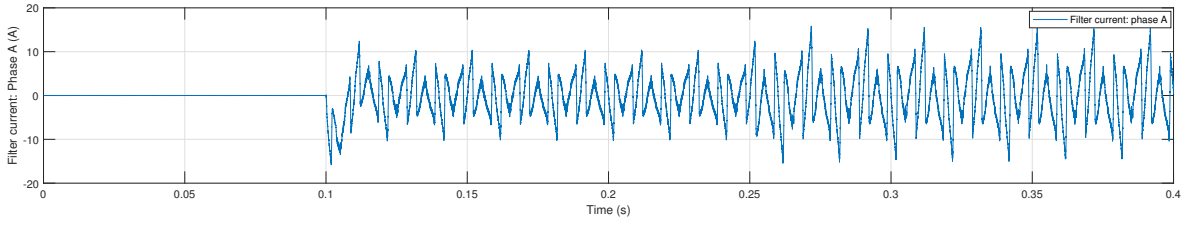
(b) PLL voltage: proposed VOC-SVM



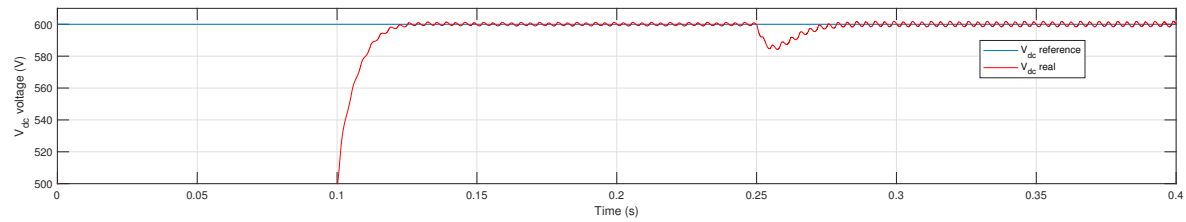
(c) Source current: proposed VOC-SVM



(d) Load current: proposed VOC-SVM

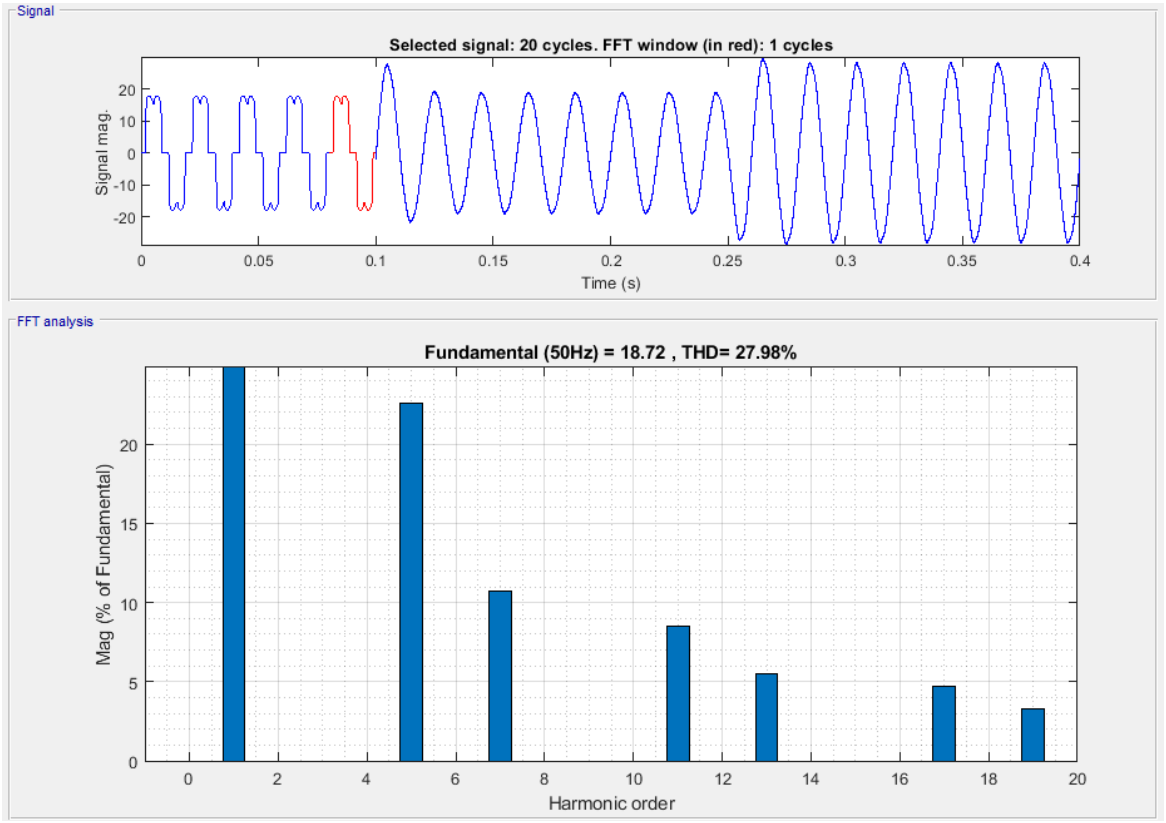


(e) Filter current: proposed VOC-SVM

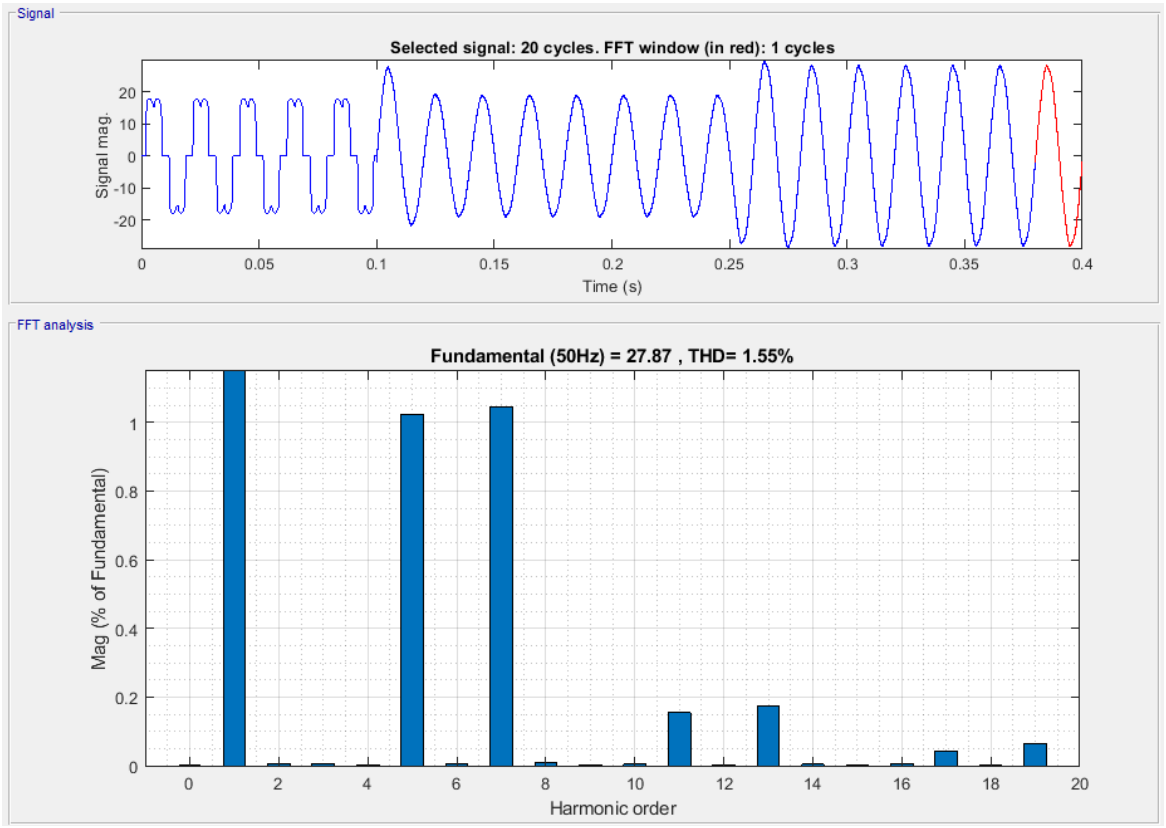


(f) Bus voltage: proposed VOC-SVM

Fig. 11. Results of the transient for a variable nonlinear load when the SAPF is closed at t=0.1s

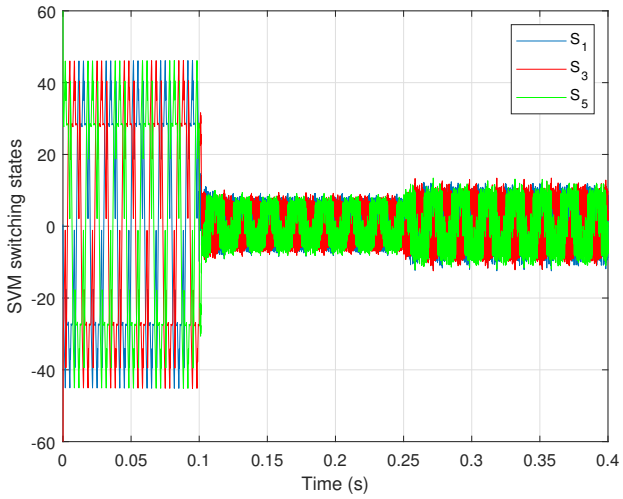


(a) Before filter closure

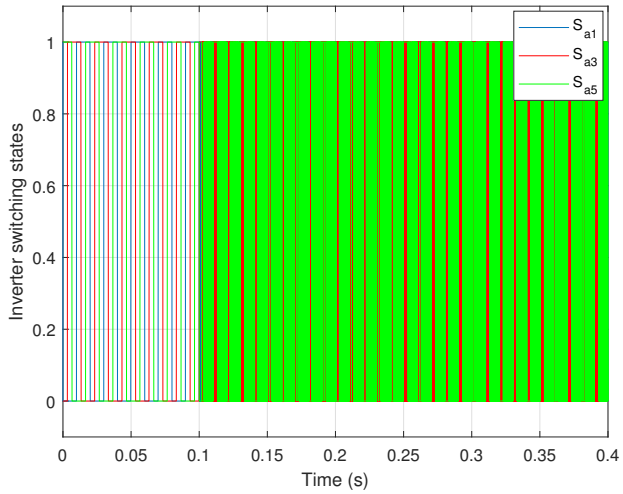


(b) After filter closure

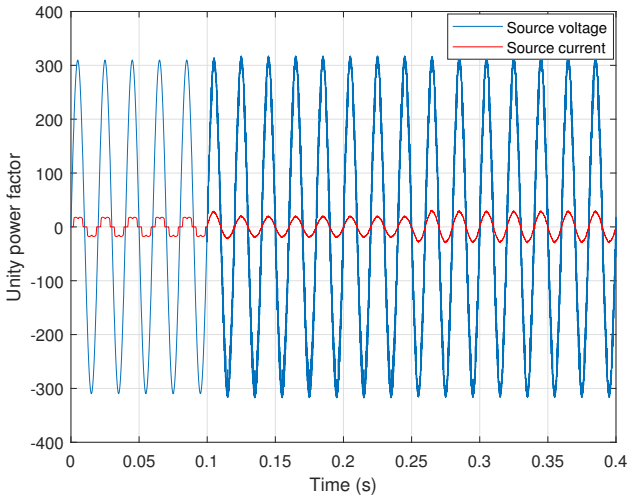
Fig. 12. Spectra of the source current after and before filtering



(a) SVM switching state



(b) Inverter switching state



(c) Unity power factor

Fig. 13. Proposed VOC-SVM high performance

5.2.2 Filtering Effectiveness

Fig. 11(c) proves that before filtering, and because of the non-linear load, the network current was not sinusoidal. After filtering, the network current becomes quasi-sinusoidal which demonstrates the effectiveness of the suggested control scheme. Fig. 11(d) shows that after closing the SAPF the load current increased because the load resistance value is reduced to half. Fig. 11(e) shows the filter current waveform to compensate for the reactive power after closing the SAPF.

The DC voltage in Fig. 11(f) tracks its reference (V_{dc}^{*}=600V) during only 5×10^{-2} seconds and keeps its stability over the steady state, this response time confirms the robustness of the suggested control. The load variation affects little its tracking which proves the robustness of the antiwindup regulator in the V_{dc} regulation loop.

The DC bus voltage follows its reference but fluctuations are apparent, which proves that the SAPF does indeed deliver inverse current components which are otherwise absorbed by the load. These fluctuations propagate also on the reference of the direct component of the current i_{ds}^{*}. In the final analysis, it is remarkable that the active power is not constant and also oscillates around its average value. The same goes for the reactive power which fluctuates around a zero average value and therefore takes positive and negative values. The SAPF succeeds in perfectly compensating the reactive power and its beneficial action on the re-balancing of voltages and currents as well as on harmonic pollution reduction.

5.2.3 THD Analysis

Fig. 12 highlights the analysis of the network's current THD before and after the filter closure. The THD value was **27.98**% Fig. 12(a) and it becomes **1.55**% Fig. 12(b), which indicates total conformity with the **IEEE 519-1992** standard.

5.2.4 SVM Performance

On the other hand, Fig. 13(a) shows the SVM switching states. Their magnitudes decrease and become quasi-sinusoidal immediately after the filter closure. Fig. 13(b) shows the inverter switching states. Their waveforms become uniform immediately after the filter closure. Fig. 13(c) proves the network voltage and current synchronization, which achieves a unitary power factor.

5.2.5 Control Robustness

Fig. 11(c) demonstrates that the current inrush in accordance with the load variation is instantaneous, and suffering no distortion. But making a decrease in the DC-link voltage Fig. 11(f). It should be recorded that the proposed VOC-SVM is robust, the proof is the excellent tracking of the DC voltage to its reference.

It should be noted that the currents supplied by the filter reach values comparable to the currents consumed by the polluting load. In this case, the SAPF and the load have then powers of the same order of magnitude.

6. Conclusion

To surmount the disadvantages and limitations of the conventional voltage oriented-control, a detailed conception and investigation of a new version-based SVM and robust PLL are presented in this research. The main goal is to achieve these points:

- Amelioration of instantaneous powers basing on the electrical model in the synchronous reference frame.
- Setting out a robust control based on the reactive and active powers for numerous voltage vectors based on the numerical SVM algorithm.
- Defining a new PLL structure-based BPMVF.

The validation of the suggested SAPF-VOC using the SVM algorithm was realized under MATLAB/Simulink. Many simulation attempts are carried out to affirm the control strategy's high performance, showing that the source current which wasn't sinusoidal (THD=27.98%) will become quasi-sinusoidal (THD=1.55%) after the SAPF closer. The reactive power is null on average guarantying thus a unitary power factor. The transient regime proves the control robustness by showing perfect performance either of overshoot or stability.

For the continuity of the research, the proposed method can be improved by inserting sliding mode controllers in the outer DC-link loop and inner current loops.

Author Contribution: Bouchaib Essoussi: Conceptualization, Methodology, Software. Ahmed Moutabir: Data curation, Writing-Original draft preparation. Bahloul Bensassi: Visualization, Investigation. Abderrahmane Ouchatti: Supervision. Yassine Zahraoui: Software, Validation. Bouchaib Benazza: Writing-Reviewing and Editing.

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